

MITSUBISHI MICROCOMPUTERS

M37221EF-XXXSP, M37221EFSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37221EF-XXXSP and M37221EFSP are single-chip microcomputers designed with CMOS silicon gate technology. They are housed in a 42-pin shrink plastic molded DIP.

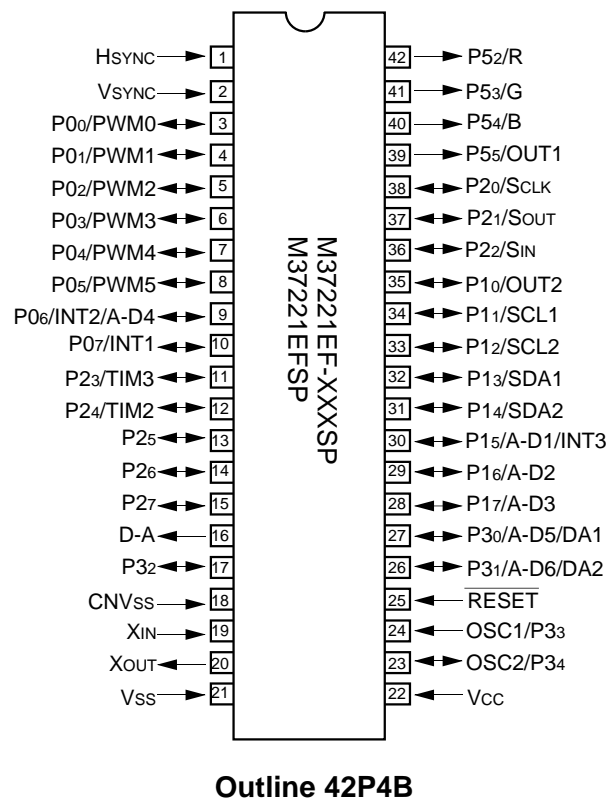
In addition to their simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

The M37221EF-XXXSP and M37221EFSP have a PWM output function and a OSD display function, so it is useful for a channel selection system for TV.

FEATURES

- Number of basic instructions 71
- Memory size
 - ROM 62 K bytes
 - RAM 1216 bytes
 - ROM for display 8 K bytes
 - RAM for display 96 bytes
- The minimum instruction execution time
 - 0.5 μ s (at 8 MHz oscillation frequency)
- Power source voltage 5 V \pm 10 %
- Power dissipation 165 mW
(at 8 MHz oscillation frequency, V_{CC}=5.5V, at CRT display)
- Subroutine nesting 96 levels (maximum)
- Interrupts 14 types, 14 vectors
- 8-bit timers 4
- Programmable I/O ports (Ports P0, P1, P2, P30-P32) 27
- Input ports (Ports P33, P34) 2
- Output ports (Ports P52-P55) 4
- 12 V withstand ports 6
- LED drive ports 4
- Serial I/O 8-bit \times 1 channel
- Multi-master I²C-BUS interface 1 (2 systems)
- A-D comparator (6-bit resolution) 6 channels
- D-A converter (6-bit resolution) 2
- PWM output circuit 14-bit \times 1, 8-bit \times 6
- ROM correction function 32 bytes \times 2

PIN CONFIGURATION (TOP VIEW)



- CRT display function
 - Number of display characters 24 characters \times 2 lines
(16 lines maximum)
 - Kinds of characters 256 kinds
 - Dot structure 12 \times 16 dots
 - Kinds of character sizes 3 kinds
 - Kinds of character colors (It can be specified by the character)
maximum 7 kinds (R, G, B)
 - Kinds of character background colors (It can be specified by the character)
maximum 7 kinds (R, G, B)
 - Kinds of raster colors (maximum 7 kinds)
 - Display position
 - Horizontal 64 levels
 - Vertical 128 levels
 - Bordering (horizontal and vertical)

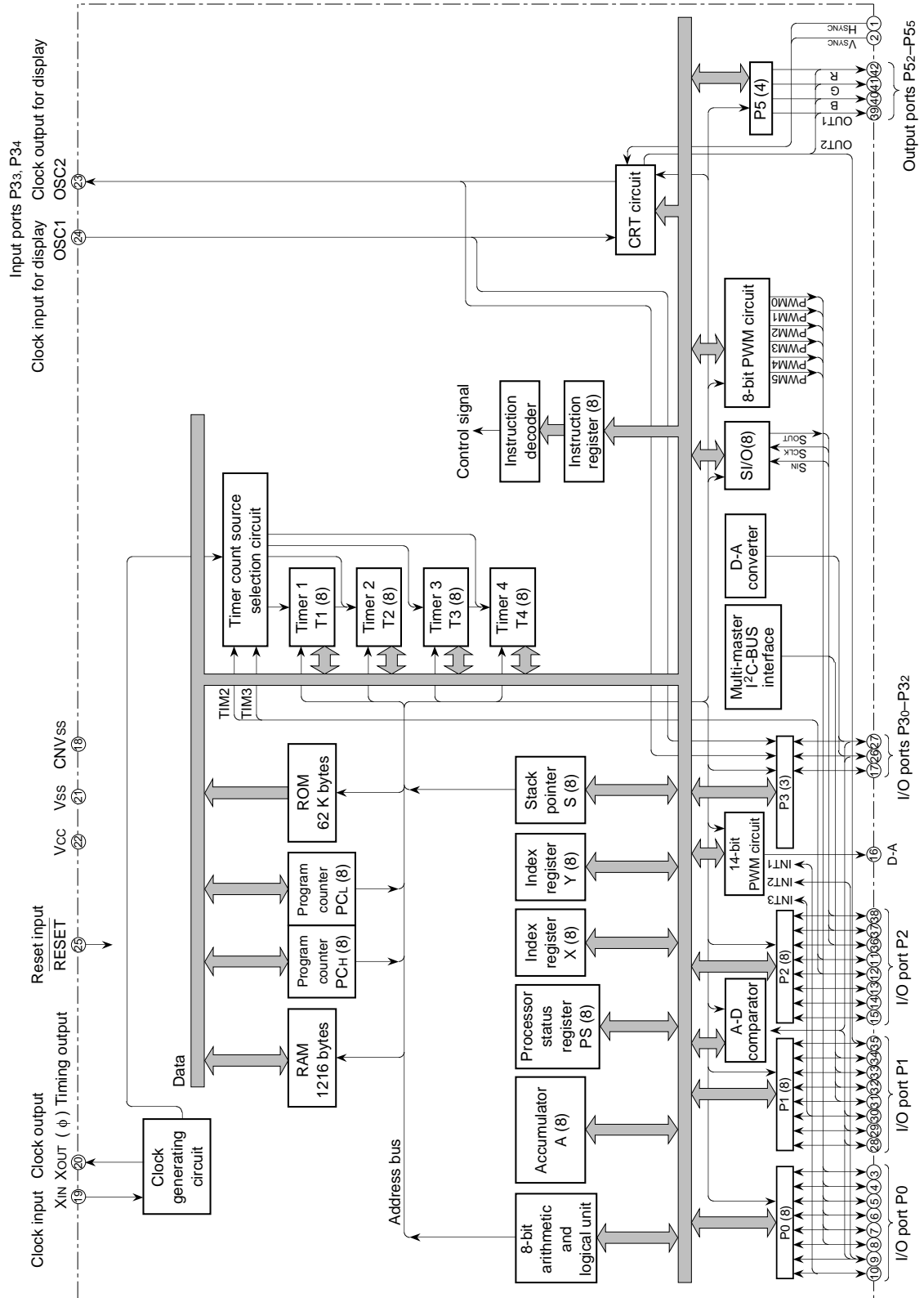
APPLICATION

TV

M37221EF-XXXSP, M37221EFSP

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FUNCTIONAL BLOCK DIAGRAM of M37221EF-XXXSP



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FUNCTIONS

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 μ s (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM		62 K bytes
	RAM		1216 bytes
	CRT ROM		8 K bytes
	CRT RAM		96 bytes
Input/Output ports	P0	I/O	8-bit \times 1 (N-channel open-drain output structure, can be used as PWM output pins, INT input pins, A-D input pin)
	P10, P15–P17	I/O	4-bit \times 1 (CMOS input/output structure, can be used as CRT output pin, A-D input pins, INT input pin)
	P11–P14	I/O	4-bit \times 1 (CMOS input/output structure, can be used as multi-master I ² C-BUS interface)
	P20, P21	I/O	2-bit \times 1 (CMOS input/output or N-channel open-drain output structure, can be used as serial I/O pins)
	P22–P27	I/O	6-bit \times 1 (CMOS input/output structure, can be used as serial input pin, external clock input pins)
	P30, P31	I/O	2-bit \times 1 (CMOS input/output or N-channel open-drain output structure, can be used as A-D input pins, D-A conversion output pins)
	P32	I/O	1-bit \times 1 (N-channel open-drain output structure)
	P33, P34	Input	2-bit \times 1 (can be used as CRT display clock I/O pins)
	P52–P55	Output	4-bit \times 1 (CMOS output structure, can be used as CRT output pins)
Serial I/O			8-bit \times 1
Multi-master I ² C-BUS interface			1 (2 systems)
A-D comparator			6 channels (6-bit resolution)
D-A converter			2 (6-bit resolution)
PWM output circuit			14-bit \times 1, 8-bit \times 6
Timers			8-bit timer \times 4
ROM correction function			32 bytes \times 2
Subroutine nesting			96 levels (maximum)
Interrupt			External interrupt \times 3, Internal timer interrupt \times 4, Serial I/O interrupt \times 1, CRT interrupt \times 1, Multi-master I ² C-BUS interface interrupt \times 1, f(XIN)/4096 interrupt \times 1, VSYNC interrupt \times 1, BRK interrupt \times 1
Clock generating circuit			2 built-in circuits (externally connected a ceramic resonator or a quartz-crystal oscillator)
Power source voltage			5 V \pm 10 %
Power dissipation	CRT ON		165 mW typ. (at oscillation frequency f _{CPU} = 8 MHz, f _{CRT} = 8 MHz)
	CRT OFF		110 mW typ. (at oscillation frequency f _{CPU} = 8 MHz)
	In stop mode		1.65 mW (maximum)
Operating temperature range			–10 °C to 70 °C
Device structure			CMOS silicon gate process
Package			42-pin shrink plastic molded DIP
CRT display function	Number of display characters		24 characters \times 2 lines (maximum 16 lines by software)
	Dot structure		12 \times 16 dots
	Kinds of characters		256 kinds
	Kinds of character sizes		3 kinds
	Kinds of character colors		Maximum 7 kinds (R, G, B); can be specified by the character
	Display position (horizontal, vertical)		64 levels (horizontal) \times 128 levels (vertical)

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
VCC, VSS.	Power source		Apply voltage of $5\text{ V} \pm 10\%$ (typical) to VCC, and 0 V to VSS.
CNVss	CNVss		This is connected to VSS.
RESET	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2 μs or more (under normal VCC conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
P00/PWM0– P05/PWM5, P06/INT2/ A-D4, P07/INT1	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open-drain output. The note out of this Table gives a full of port P0 function.
	PWM output	Output	Pins P00–P05 are also used as PWM output pins PWM0–PWM5 respectively. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pins P06, P07 are also used as external interrupt input pins INT2, INT1 respectively.
	Analog input	Input	P06 pin is also used as analog input pin A-D4.
P10/OUT2, P11/SCL1, P12/SCL2, P13/SDA1, P14/SDA2, P15/A-D1/ INT3, P16/A-D2, P17/A-D3	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	CRT output	Output	Pins P10 is also used as CRT output pin OUT2. The output structure is CMOS output.
	Multi-master I ² C-BUS interface	I/O	Pins P11–P14 are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I ² C-BUS interface is used. The output structure is N-channel open-drain output.
	Analog input	Input	Pins P15–P17 are also used as analog input pins A-D1 to A-D3 respectively.
	External interrupt input	Input	P15 pin is also used as external interrupt input pin INT3.
P20/SCLK, P21/SOUT, P22/SIN, P23/TIM3, P24/TIM2, P25–P27	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	External clock input	Input	Pins P23, P24 are also used as external clock input pins TIM3, TIM2 respectively.
	Serial I/O synchronizing clock input/output	I/O	P20 pin is also used as serial I/O synchronizing clock input/output pin SCLK. The output structure is N-channel open-drain output.
	Serial I/O data input/output	I/O	Pins P21, P22 are also used as serial I/O data input/output pins SOUT, SIN respectively. The output structure is N-channel open-drain output.
P30/A-D5/ DA1, P31/A-D6/ DA2, P32	I/O port P3	I/O	Ports P30–P32 are a 3-bit I/O port and has basically the same functions as port P0. Either CMOS output or N-channel open-drain output structure can be selected as the port P30 and P31. The output structure of port P32 is N-channel open-drain output.
	Analog input	Input	Pins P30, P31 are also used as analog input pins A-D5, A-D6 respectively.
	D-A conversion output	Output	Pins P30, P31 are also used as D-A conversion output pins DA1, DA2 respectively.
P33/OSC1, P34/OSC2	Input port P3	Input	Ports P33, P34 are a 2-bit input port.
	Clock input for CRT display	Input	P33 pin is also used as CRT display clock input pin OSC1.
	Clock output for CRT display	Output	P34 pin is also used as CRT display clock output pin OSC2. The output structure is CMOS output.

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PIN DESCRIPTION (continued)

P52/R, P53/G, P54/B, P55/OUT1	Output port P5	Output	Ports P52–P55 are a 4-bit output port. The output structure is CMOS output.
	CRT output	Output	Pins P52–P55 are also used as CRT output pins R, G, B, OUT1 respectively. The output structure is CMOS output.
Hsync	Hsync input	Input	This is a horizontal synchronizing signal input for CRT.
Vsync	Vsync input	Input	This is a vertical synchronizing signal input for CRT.
D-A	DA output	Output	This is a 14-bit PWM output pin.

Note : As shown in the memory map (Figure 3), port P0 is accessed as a memory at address 00C0₁₆ of zero page. Port P0 has the port P0 direction register (address 00C1₁₆ of zero page) which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output "L" voltage has risen, for example, because a light emitting diode was directly driven. The input pins are in the floating state, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

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FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37221EF-XXXSP uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

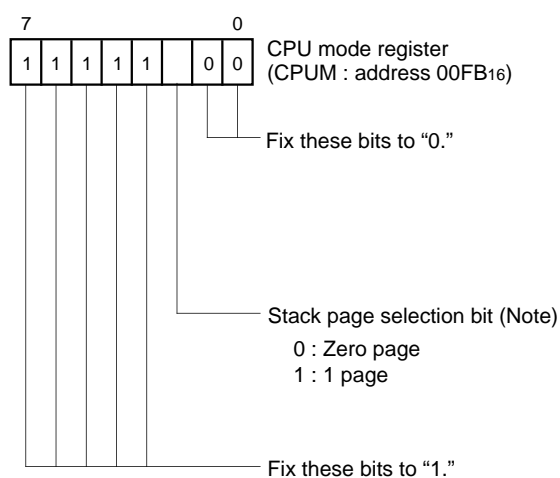
Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register contains the stack page selection bit. The CPU mode register is allocated at address 00FB₁₆.



Note : Please beware of this bit when programming because it is set to "1" after the reset release.

Fig. 1. Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

ROM is used for storing user programs as well as the interrupt vector area.

RAM for Display

RAM for display is used for specifying the character codes and colors to display.

ROM for Display

ROM for display is used for storing character data.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

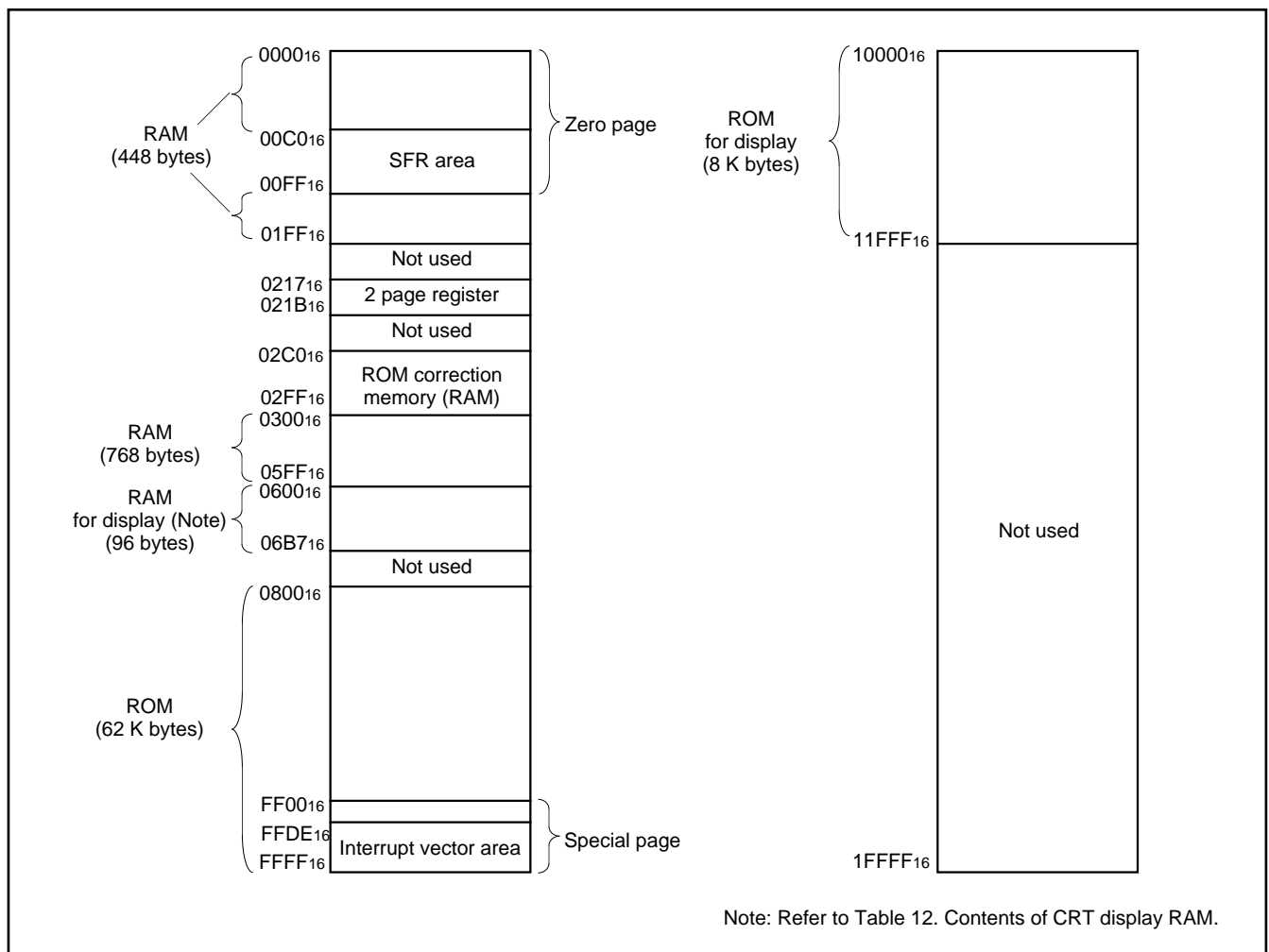


Fig. 2. Memory map

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■SFR area (addresses C0₁₆ to DF₁₆)

□ : Nothing is allocated

▨ : Fix this bit to "0" (do not write "1")

0 : "0" immediately after reset

1 : "1" immediately after reset

? : undefined immediately after reset







Address	Register	Bit allocation	State immediately after reset
		b7 b0	b7 b0
C0 ₁₆	Port P0 (P0)		?
C1 ₁₆	Port P0 direction register (D0)		00 ₁₆
C2 ₁₆	Port P1 (P1)		?
C3 ₁₆	Port P1 direction register (D1)		00 ₁₆
C4 ₁₆	Port P2 (P2)		?
C5 ₁₆	Port P2 direction register (D2)		00 ₁₆
C6 ₁₆	Port P3 (P3)		0 0 0 ? ? ? ? ?
C7 ₁₆	Port P3 direction register (D3)		0 0 0 0 0 0 0 0
C8 ₁₆			?
C9 ₁₆			?
CA ₁₆	Port P5 (P5)		0 0 ? ? ? ? ? ?
CB ₁₆	Port P5 direction register (D5)		0 0 0 0 0 0 0 0
CC ₁₆			?
CD ₁₆	Port P3 output mode control register (P3S)	DA2S DA1S P31S P30S	0 0 0 0 0 0 0 0
CE ₁₆	DA-H register (DA-H)		?
CF ₁₆	DA-L register (DA-L)		0 0 ? ? ? ? ? ?
D0 ₁₆	PWM0 register (PWM0)		?
D1 ₁₆	PWM1 register (PWM1)		?
D2 ₁₆	PWM2 register (PWM2)		?
D3 ₁₆	PWM3 register (PWM3)		?
D4 ₁₆	PWM4 register (PWM4)		?
D5 ₁₆	PWM output control register 1 (PW)	PW7 PW6 PW5 PW4 PW3 PW2 PW1 PW0	00 ₁₆
D6 ₁₆	PWM output control register 2 (PN)	PN4 PN3 PN2	0 0 0 0 0 0 0 0
D7 ₁₆	I ² C data shift register (S0)		?
D8 ₁₆	I ² C address register (S0D)	SAD6 SAD5 SAD4 SAD3 SAD2 SAD1 SAD0 RBW	00 ₁₆
D9 ₁₆	I ² C status register (S1)	MST TRX BB PIN AL AAS AD0 LRB	0 0 0 1 0 0 0 ?
DA ₁₆	I ² C control register (S1D)	BSEL1 BSEL0 10 BIT SAD ALS ES0 BC2 BC1 BC0	00 ₁₆
DB ₁₆	I ² C clock control register (S2)	ACK ACK BIT FAST MODE CCR4 CCR3 CCR2 CCR1 CCR0	00 ₁₆
DC ₁₆	Serial I/O mode register (SM)	SM6 SM5 SM3 SM2 SM1 SM0	0 0 0 0 0 0 0 0
DD ₁₆	Serial I/O register (SIO)		?
DE ₁₆	DA1 conversion register (DA1)	DA15 DA14 DA13 DA12 DA11 DA10	0 0 ? ? ? ? ? ?
DF ₁₆	DA2 conversion register (DA2)	DA25 DA24 DA23 DA22 DA21 DA20	0 0 ? ? ? ? ? ?

Fig. 3. Memory map of SFR (special function register) (1)

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■SFR area (addresses E0₁₆ to FF₁₆)

-  : Nothing is allocated
 : Fix this bit to "0" (do not write "1")
 : Fix this bit to "1" (do not write "0")
 : "0" immediately after reset
 : "1" immediately after reset
 : undefined immediately after reset

















Address	Register	Bit allocation								State immediately after reset							
		b7								b0							
E0 ₁₆	Horizontal register (HR)			HR5	HR4	HR3	HR2	HR1	HR0	0	0	0	0	0	0	0	0
E1 ₁₆	Vertical register 1 (CV1)		CV16	CV15	CV14	CV13	CV12	CV11	CV10	0	?	?	?	?	?	?	?
E2 ₁₆	Vertical register 2 (CV2)		CV26	CV25	CV24	CV23	CV22	CV21	CV20	0	?	?	?	?	?	?	?
E3 ₁₆										?							
E4 ₁₆	Character size register (CS)					CS21	CS20	CS11	CS10	0	0	0	0	?	?	?	?
E5 ₁₆	Border selection register (MD)						MD20		MD10	0	0	0	0	0	?	0	?
E6 ₁₆	Color register 0 (CO0)	CO07	CO06	CO05	CO04	CO03	CO02	CO01		0	0	0	0	0	0	0	0
E7 ₁₆	Color register 1 (CO1)	CO17	CO16	CO15	CO14	CO13	CO12	CO11		0	0	0	0	0	0	0	0
E8 ₁₆	Color register 2 (CO2)	CO27	CO26	CO25	CO24	CO23	CO22	CO21		0	0	0	0	0	0	0	0
E9 ₁₆	Color register 3 (CO3)	CO37	CO36	CO35	CO34	CO33	CO32	CO31		0	0	0	0	0	0	0	0
EA ₁₆	CRT control register (CC)	CC7					CC2	CC1	CC0	0	0	0	0	0	0	0	0
EB ₁₆										?							
EC ₁₆	CRT port control register (CRTP)	OP7	OP6	OP5	OUT1	OUT2	R/G/B	VSYN	HSYN	00 ₁₆							
ED ₁₆	CRT clock selection register (CK)							CK1	CK0						0	0	
EE ₁₆	A-D control register 1 (AD1)				ADM4		ADM2	ADM1	ADM0	0	0	0	?	0	0	0	0
EF ₁₆	A-D control register 2 (AD2)			ADC5	ADC4	ADC3	ADC2	ADC1	ADC0	0	0	0	0	0	0	0	0
F0 ₁₆	Timer 1 (TM1)									FF ₁₆							
F1 ₁₆	Timer 2 (TM2)									07 ₁₆							
F2 ₁₆	Timer 3 (TM3)									FF ₁₆							
F3 ₁₆	Timer 4 (TM4)									07 ₁₆							
F4 ₁₆	Timer 12 mode register (T12M)				T12M4	T12M3	T12M2	T12M1	T12M0	0	0		0	0	0	0	0
F5 ₁₆	Timer 34 mode register (T34M)			T34M5	T34M4	T34M3	T34M2	T34M1	T34M0	0	0	0	0	0	0	0	0
F6 ₁₆	PWM5 register (PWM5)									?							
F7 ₁₆										?							
F8 ₁₆										?							
F9 ₁₆	Interrupt input polarity register (RE)			RE5	RE4	RE3					0	0	0	0	0		?
FA ₁₆	Test register (TEST)																
FB ₁₆	CPU mode register (CPUM)						CM2								1	0	0
FC ₁₆	Interrupt request register 1 (IREQ1)	IT3R	IICR	VSCR	CRTR	TM4R	TM3R	TM2R	TM1R	0	0	0	0	0	0	0	0
FD ₁₆	Interrupt request register 2 (IREQ2)				MSR		S1R	1T2R	1T1R		0	0	0	0	0	0	0
FE ₁₆	Interrupt control register 1 (ICON1)	IT3E	IICE	VSCE	CRTE	TM4E	TM3E	TM2E	TM1E	0	0	0	0	0	0	0	0
FF ₁₆	Interrupt control register 2 (ICON2)				MSE		S1E	1T2E	1T1E		0	0	0	0	0	0	0

Fig. 4. Memory map of SFR (special function register) (2)

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■SFR area (addresses 200₁₆ to 21F₁₆)

□ : Nothing is allocated

▨ : Fix this bit to "0" (do not write "1")

0 : "0" immediately after reset

Address	Register	Bit allocation		State immediately after reset	
		b7	b0	b7	b0
200 ₁₆				?	
201 ₁₆				?	
202 ₁₆				?	
203 ₁₆				?	
204 ₁₆				?	
205 ₁₆				?	
206 ₁₆				?	
207 ₁₆				?	
208 ₁₆				?	
209 ₁₆				?	
20A ₁₆				?	
20B ₁₆				?	
20C ₁₆				?	
20D ₁₆				?	
20E ₁₆				?	
20F ₁₆				?	
210 ₁₆				?	
211 ₁₆				?	
212 ₁₆				?	
213 ₁₆				?	
214 ₁₆				?	
215 ₁₆				?	
216 ₁₆				?	
217 ₁₆	ROM correction address 1 (high-order)			?	
218 ₁₆	ROM correction address 1 (low-order)			?	
219 ₁₆	ROM correction address 2 (high-order)			?	
21A ₁₆	ROM correction address 2 (low-order)			?	
21B ₁₆	ROM correction enable register (RCR)		RCR1 RCR0	0 0 0 0 ▨ ▨ 0 0	
21C ₁₆				?	
21D ₁₆				?	
21E ₁₆				?	
21F ₁₆				?	

Fig. 5. Memory map of 2 page register

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INTERRUPTS

Interrupts can be caused by 14 different sources consisting of 4 external, 8 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

- (1) The contents of the program counter and processor status register are automatically stored into the stack.
- (2) The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
- (3) The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 7 shows the structure of the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority.

Figure 6 shows interrupt control.

Interrupt Causes

- (1) VSYNC and CRT interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.

The CRT interrupt occurs after character block display to the CRT is completed.

- (2) INT1, INT2, INT3 interrupts

With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L," and generates an interrupt request. The input active edge can be selected by bits 3, 4 and 5 of the interrupt input polarity register (address 00F9₁₆) : when this bit is "0," a change from "L" to "H" is detected; when it is "1," a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

- (3) Timer 1, 2, 3 and 4 interrupts

An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

- (4) Serial I/O interrupt

This is an interrupt request from the clock synchronous serial I/O function.

Table 1. Interrupt vector addresses and priority

Interrupt source	Priority	Vector addresses	Remarks
Reset	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT2 interrupt	3	FFFB ₁₆ , FFFA ₁₆	Active edge selectable
INT1 interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	Active edge selectable
Timer 4 interrupt	5	FFF5 ₁₆ , FFF4 ₁₆	
f(XIN)/4096 interrupt	6	FFF3 ₁₆ , FFF2 ₁₆	
VSYNC interrupt	7	FFF1 ₁₆ , FFF0 ₁₆	Active edge selectable
Timer 3 interrupt	8	FFEF ₁₆ , FFEE ₁₆	
Timer 2 interrupt	9	FFED ₁₆ , FFEC ₁₆	
Timer 1 interrupt	10	FFEB ₁₆ , FFEA ₁₆	
Serial I/O interrupt	11	FFE9 ₁₆ , FFE8 ₁₆	
Multi-master I ² C-BUS interface interrupt	12	FFE7 ₁₆ , FFE6 ₁₆	
INT3 interrupt	13	FFE5 ₁₆ , FFE4 ₁₆	Active edge selectable
BRK instruction interrupt	14	FFDF ₁₆ , FFDE ₁₆	Non-maskable (software interrupt)

- (5) $f(X_{IN})/4096$ interrupt
This interrupt occurs regularly with a $f(X_{IN})/4096$ period. Set bit 0 of the PWM output control register 1 to "0."
- (6) Multi-master I²C-BUS interface interrupt
This is an interrupt related to the multi-master I²C-BUS interface.
- (7) BRK instruction interrupt
This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

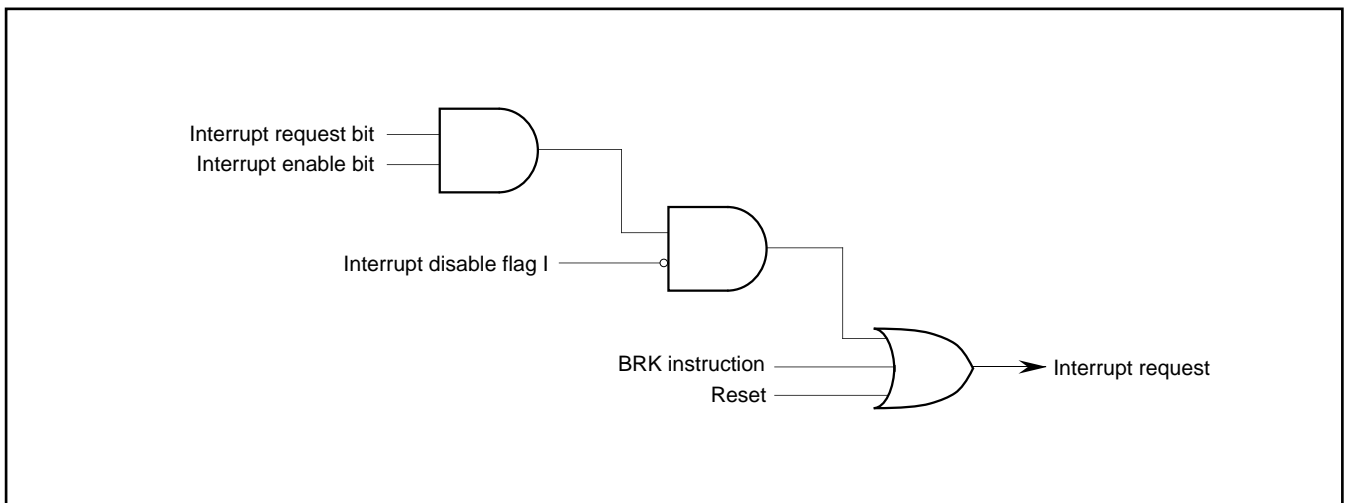


Fig. 6. Interrupt control

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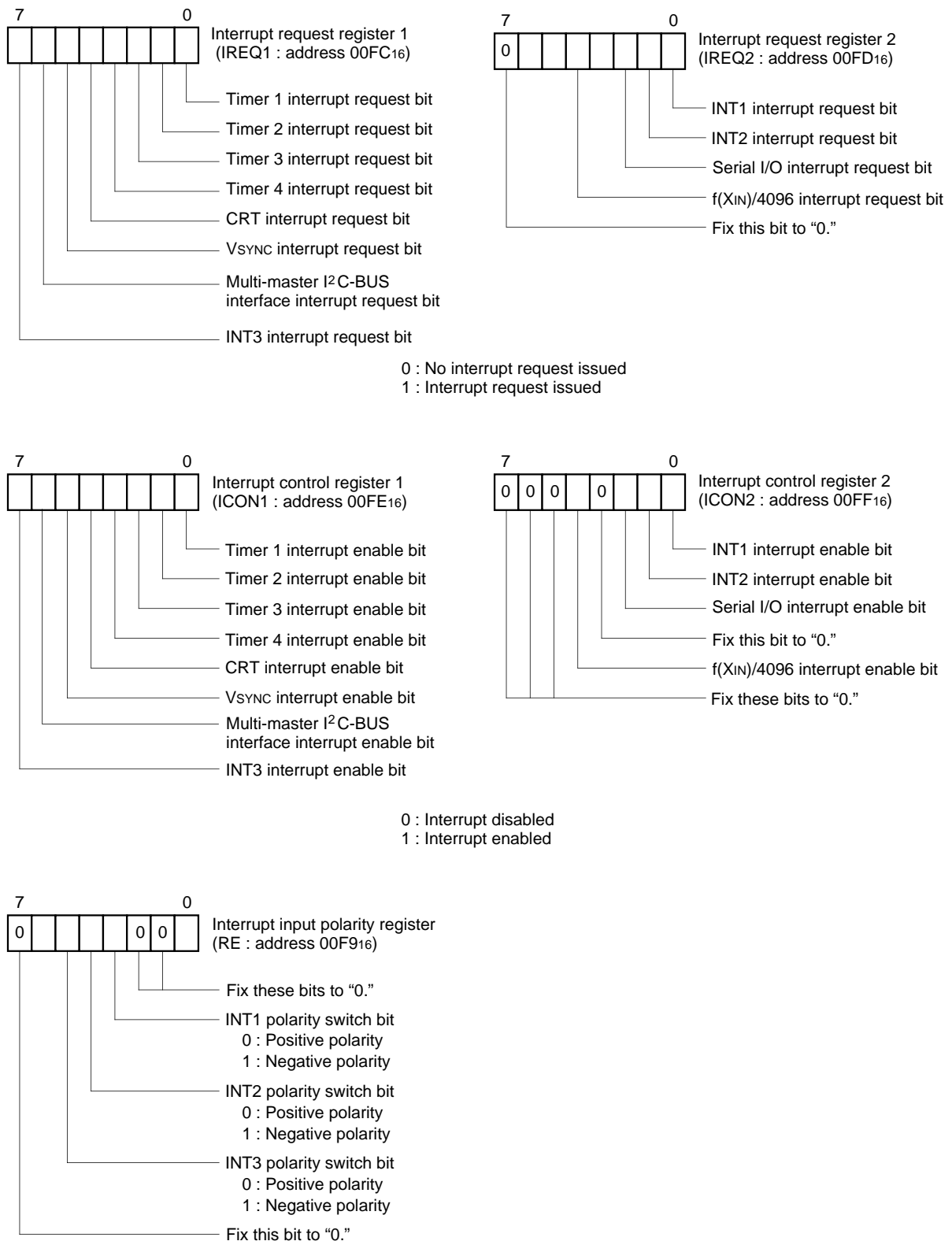


Fig. 7. Structure of interrupt-related registers

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TIMERS

The M37221EF-XXXSP has 4 timers: timer 1, timer 2, timer 3, and timer 4. All timers are 8-bit timer with the 8-bit timer latch. The timer block diagram is shown in Figure 9.

All of the timers count down and their divide ratio is $1/(n+1)$, where n is the value of timer latch. The value is set to a timer at the same time by writing a count value to the corresponding timer latch (addresses 00F0₁₆ to 00F3₁₆).

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse after the count value reaches "00₁₆".

(1) Timer 1

Timer 1 can select one of the following count sources:

- $f(X_{IN})/16$
- $f(X_{IN})/4096$

The count source of timer 1 is selected by setting bit 0 of the timer 12 mode register (address 00F4₁₆).

Timer 1 interrupt request occurs at timer 1 overflow.

(2) Timer 2

Timer 2 can select one of the following count sources:

- $f(X_{IN})/16$
- Timer 1 overflow signal
- External clock from the P24/TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of the timer 12 mode register (address 00F4₁₆). When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- $f(X_{IN})/16$
- External clock from the HSYNC pin
- External clock from the P23/TIM3 pin

The count source of timer 3 is selected by setting bits 5 and 0 of the timer 34 mode register (address 00F5₁₆).

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- $f(X_{IN})/16$
- $f(X_{IN})/2$
- Timer 3 overflow signal

The count source of timer 4 is selected by setting bits 4 and 1 of the timer 34 mode register (address 00F5₁₆). When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF₁₆" is automatically set in timer 3; "07₁₆" in timer 4. The $f(X_{IN})/16$ is selected as the timer 3 count source. The internal reset is released by timer 4 overflow at these state, the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF₁₆" is automatically set in timer 3; "07₁₆" in timer 4. However, the $f(X_{IN})/16$ is not selected as the timer 3 count source. So set bit 0 of the timer 34 mode register (address 00F5₁₆) to "0" before the execution of the STP instruction ($f(X_{IN})/16$ is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow at these state, the internal clock is connected.

Because of this, the program starts with the stable clock.

The structure of timer-related registers is shown in Figure 8.

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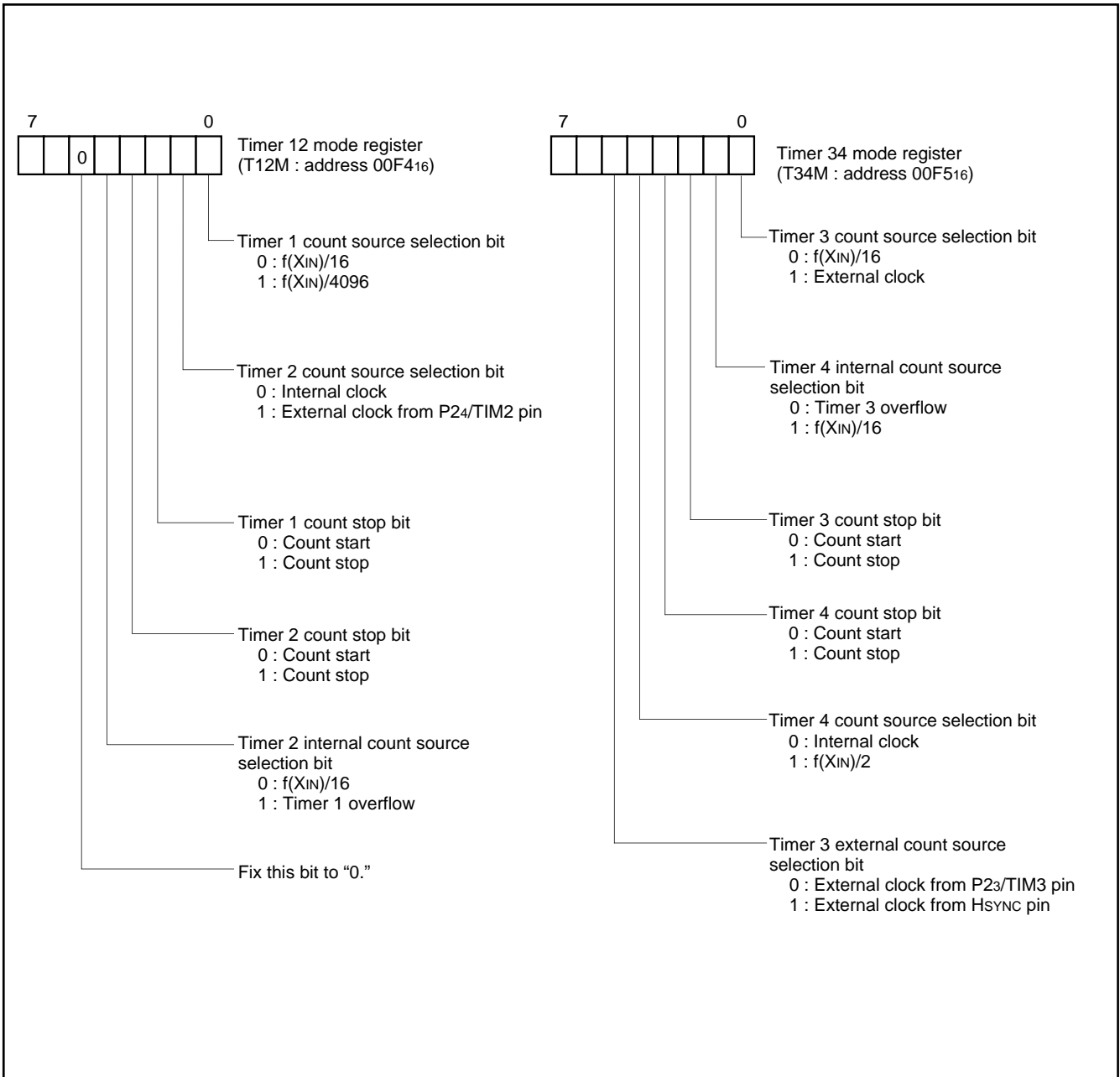


Fig. 8. Structure of timer-related registers

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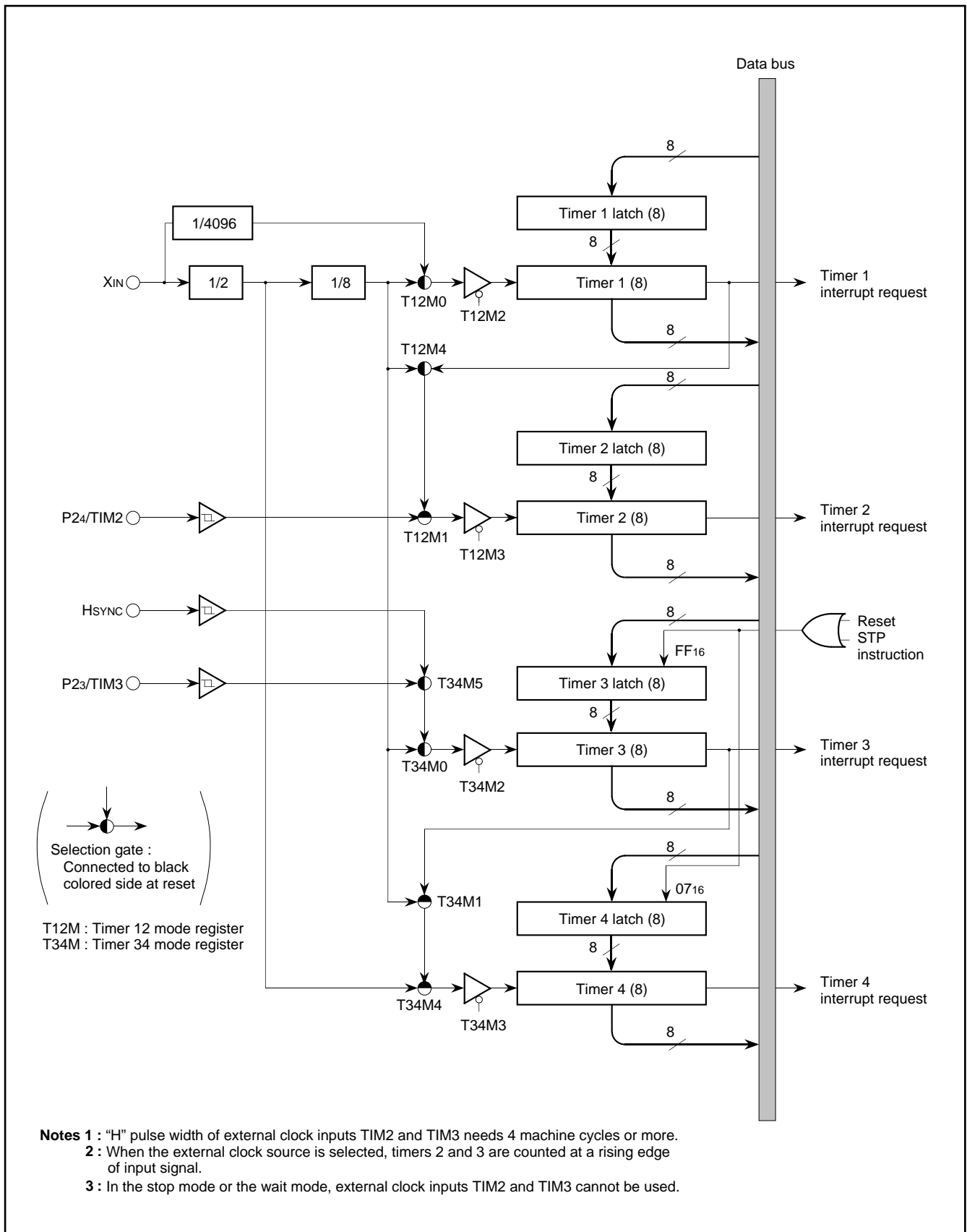


Fig. 9. Timer block diagram

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SERIAL I/O

The M37221EF-XXXSP has a built-in serial I/O which can either transmit or receive 8-bit data in serial in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 10. The synchronizing clock I/O pin (SCLK), and data I/O pins (SOUT, SIN) also function as port P2.

Bit 2 of the serial I/O mode register (address 00DC₁₆) selects whether the synchronizing clock is supplied internally or externally (from the P2₀/SCLK pin). When an internal clock is selected, bits 1 and 0 select whether $f(XIN)$ is divided by 4, 16, 32, or 64. Bit 3 selects whether port P2 is used for serial I/O or not. To use the P2₂/SIN pin as the SIN pin, set the bit 2 of the port P2 direction register (address 00C5₁₆) to "0."

The operation of the serial I/O function is described below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

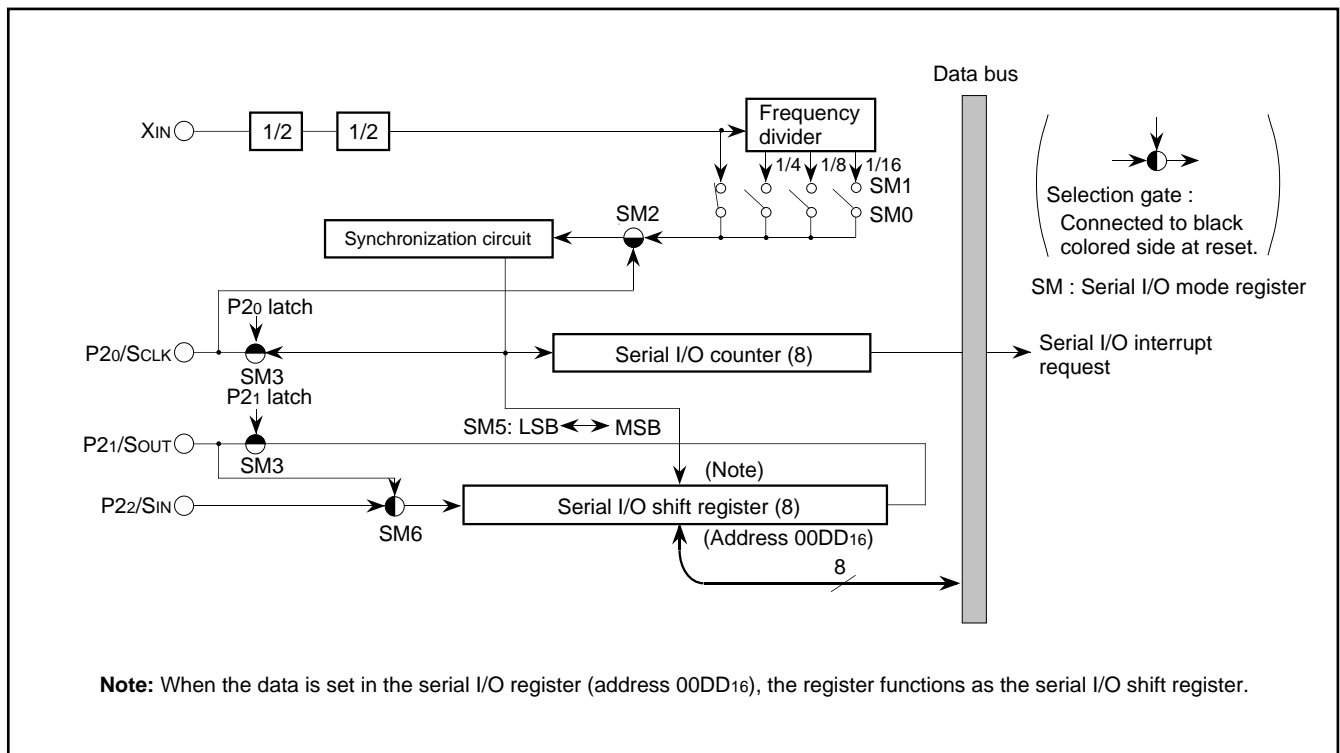


Fig. 10. Serial I/O block diagram

Internal clock—the serial I/O counter is set to “7” during write cycle into the serial I/O register (address 00DD16), and transfer clock goes “H” forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.

After the transfer clock has counted 8 times, the serial I/O counter becomes “0” and the transfer clock stops at “H.” At this time the interrupt request bit is set to “1.”

External clock—when an external clock is selected as the clock source, the interrupt request is set to “1” after the transfer clock has counted 8 times. However, transfer operation does not stop, so control the clock externally. Use the external clock of 1MHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 12. When using an external clock for transfer, the external clock must be held at “H” for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

- Notes 1:** On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions as SEB and CLB instructions.
- 2:** When an external clock is used as the synchronizing clock, write transmit data to the serial I/O register at “H” of the transfer clock input level.

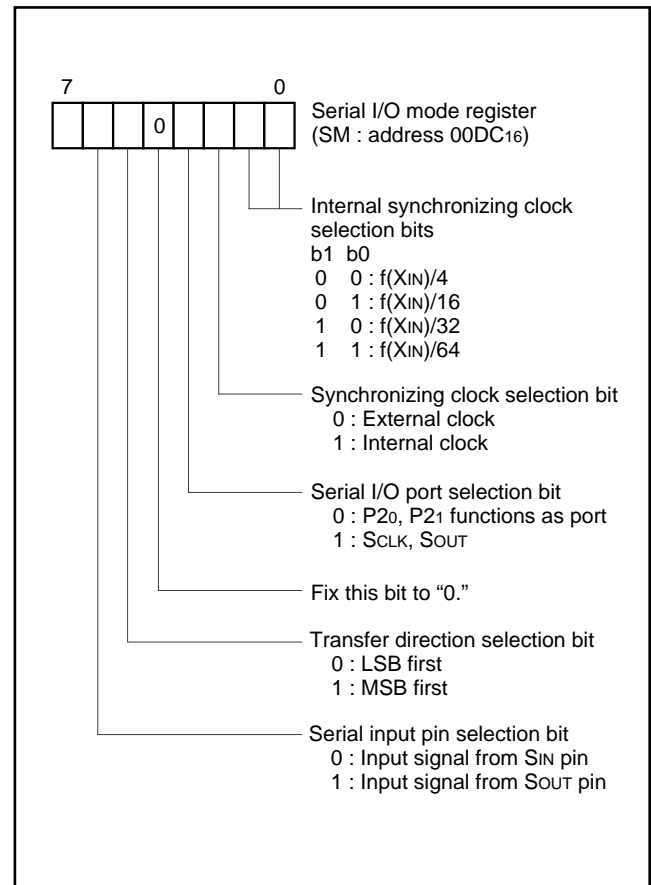


Fig. 11. Structure of serial I/O mode register

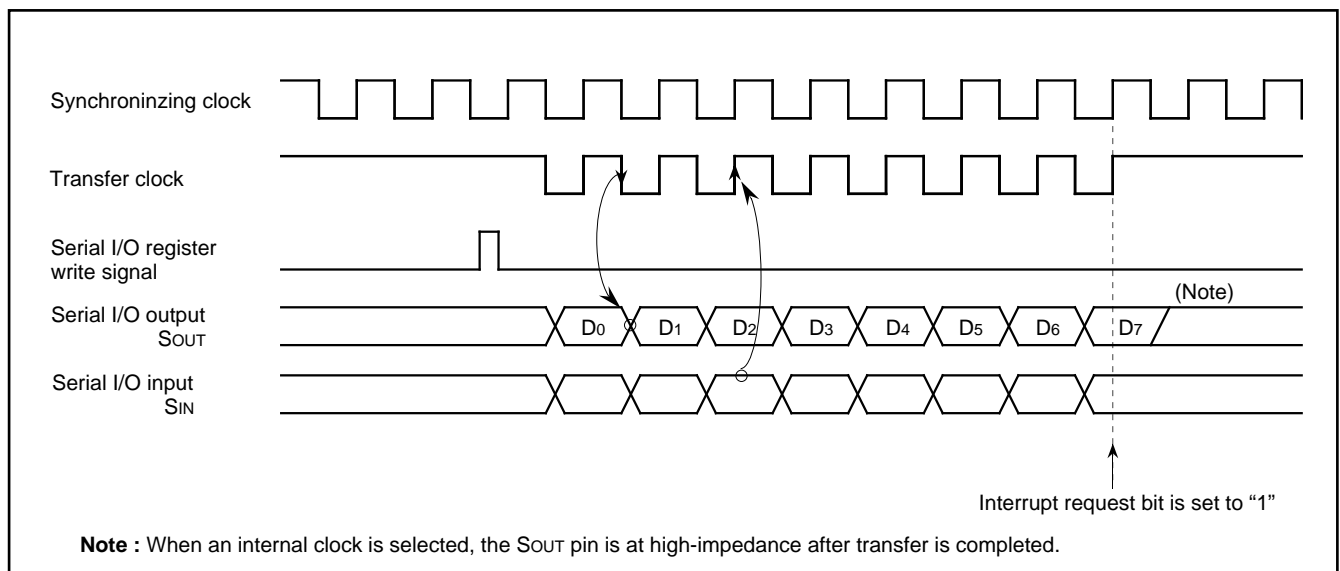


Fig. 12. Serial I/O timing (for LSB first)

Serial I/O Common Transmission/Reception Mode

By writing "1" to bit 6 of the serial I/O mode register, signals SIN and SOUT are switched internally to be able to transmit or receive the serial data.

Figure 13 shows signals on serial I/O common transmission/reception mode.

Note: When receiving the serial data after writing "FF16" to the serial I/O register.

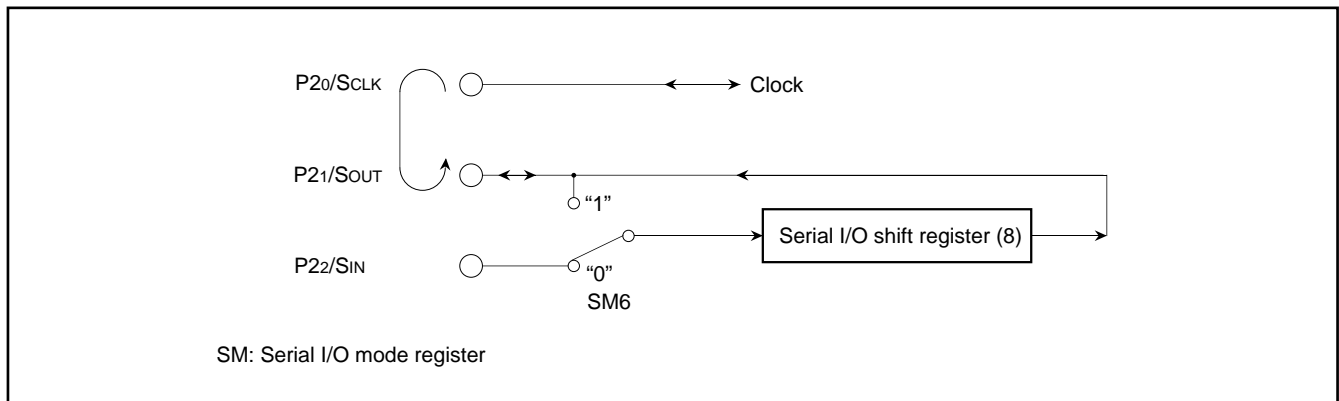


Fig. 13. Signals on serial I/O common transmission/reception mode

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MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a circuit for serial communications conformed with the Philips I²C-BUS data transfer format. This interface, having an arbitration lost detection function and a synchronous function, is useful for serial communications of the multi-master.

Figure 14 shows a block diagram of the multi-master I²C-BUS interface and Table 2 shows multi-master I²C-BUS interface functions. This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register and other control circuits.

Table 2. Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I ² C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I ² C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at $\phi = 4$ MHz)

ϕ : System clock = $f(XIN)/2$

Note: We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I²C control register at address 00DA16) for connections between the I²C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

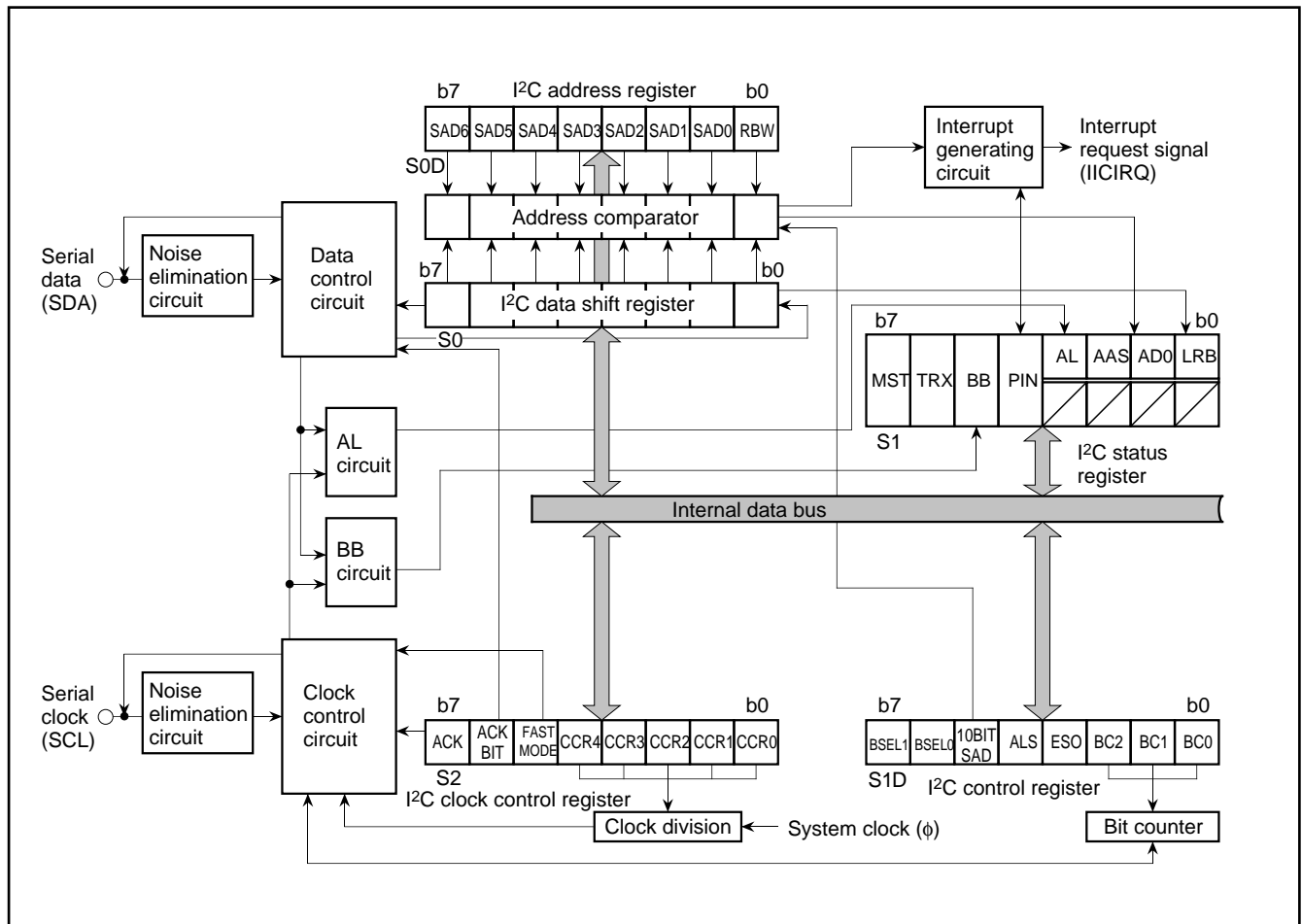


Fig. 14. Block diagram of multimaster I²C-BUS interface

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(1) I²C Data Shift Register

The I²C data shift register (S0 : address 00D7₁₆) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.

The I²C data shift register is in a write enable status only when the ES0 bit of the I²C control register (address 00DA₁₆) is "1." The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (address 00D9₁₆) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

(2) I²C Address Register

The I²C address register (address 00D8₁₆) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

■ Bit 0: Read/write bit (RBW)

Not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I²C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

■ Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

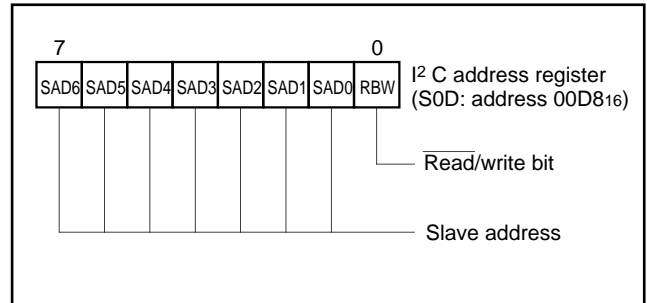


Fig. 15. Structure of I²C address register

(3) I²C Clock Control Register

The I²C clock control register (address 00DB₁₆) is used to set ACK control, SCL mode and SCL frequency.

■ Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 3.

■ Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is set. When the bit is set to "1," the high-speed clock mode is set.

■ Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is set and make SDA "L" at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is set. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address matches the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made "L" (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made "H" (ACK is not returned).

*ACK clock: Clock for acknowledgement

■ Bit 7: ACK clock bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to "0," the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmitting. If data is written during transmitting, the I²C clock generator is reset, so that data cannot be transmitted normally.

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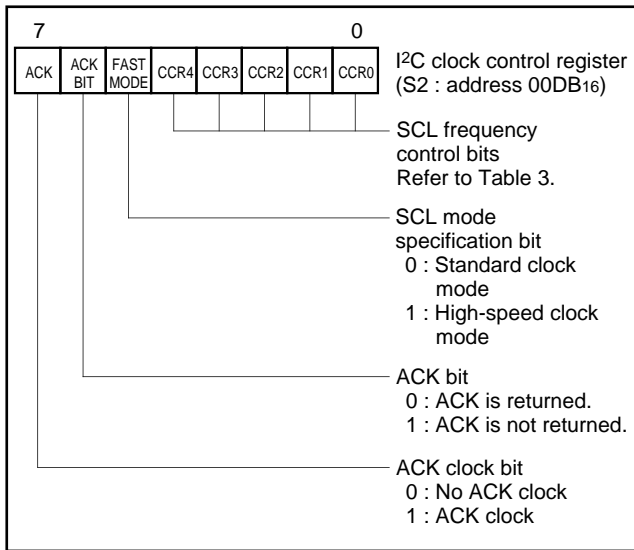


Fig. 16. Structure of I²C clock control register

Table 3. Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at $\phi = 4\text{MHz}$, unit : kHz)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	Setting disabled	333
0	0	1	0	0	Setting disabled	250
0	0	1	0	1	100	400(Note)
0	0	1	1	0	83.3	166
:	:	:	:	:	500/CCR value	1000/CCR value
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Note: At 400 kHz in the high-speed clock mode, the duty is 40%.
In the other cases, the duty is 50%.

(4) I²C Control Register

The I²C control register (address 00DA16) controls data communication format.

■ Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.

When a START condition is received, these bits become “0002” and the address data is always transmitted and received in 8 bits.

■ Bit 3: I²C interface use enable bit (ES0)

This bit enables to use the multimaster I²C BUS interface. When this bit is set to “0,” the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to “1,” use of the interface is enabled.

When ES0 = “0,” the following is performed.

- PIN = “1,” BB = “0” and AL = “0” are set (they are bits of the I²C status register at address 00D916).
- Writing data to the I²C data shift register (address 00D716) is disabled.

■ Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to “0,” the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to “(5) I²C Status Register,” bit 1) is received, transmission processing can be performed. When this bit is set to “1,” the free data format is selected, so that slave addresses are not recognized.

■ Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to “0,” the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 00D816) are compared with address data. When this bit is set to “1,” the 10-bit addressing format is selected, all the bits of the I²C address register are compared with address data.

■ Bits 6 and 7: Connection control bits between I²C-BUS interface and ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 17).

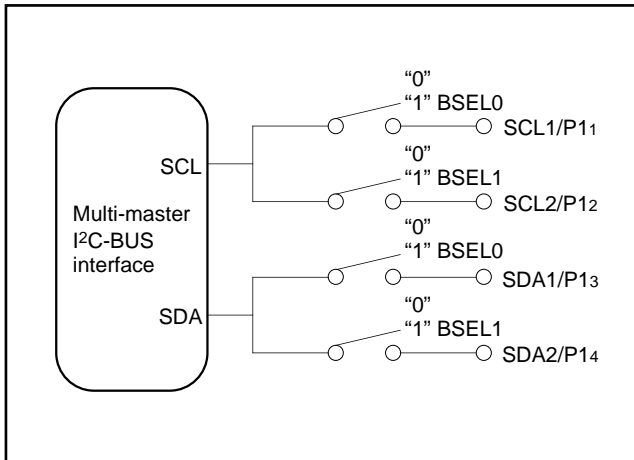


Fig. 17. Connection port control by BSEL0 and BSEL1

(5) I²C Status Register

The I²C status register (address 00D9₁₆) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

■ Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D7₁₆).

■ Bit 1: General call detecting flag (AD0)

This bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

*General call: The master transmits the general call address "00₁₆" to all slaves.

■ Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data.

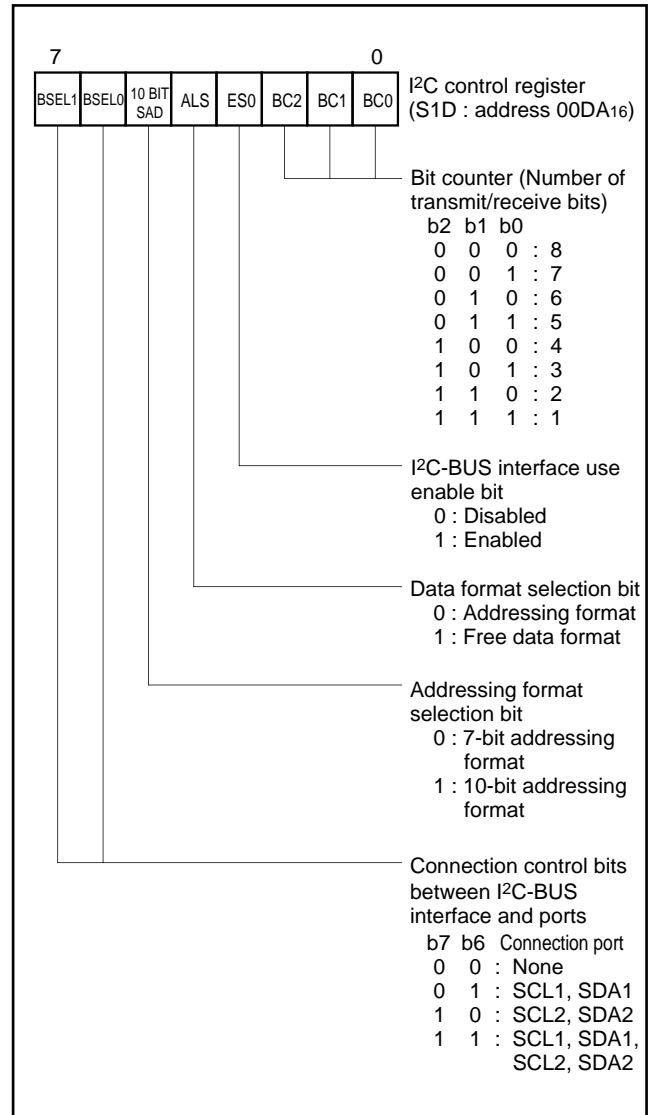
① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.

- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (address 00D8₁₆).
- A general call is received.

② In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.

- When the address data is compared with the I²C address register (8 bits consisted of slave address and RBW), the first bytes agree.

③ The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D7₁₆).


Fig. 18. Structure of I²C control register

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■ Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." In the case arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

*Arbitration lost: The status in which communication as a master is disabled.

■ Bit 4: I²C-BUS interface interrupt request bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 20 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions.

- Executing a write instruction to the I²C data shift register (address 00D7₁₆).
- When the ES0 bit is "0"
- At reset

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

■ Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (Note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ES0 bit of the I²C control register (address 00DA₁₆) is "0" and at reset, the BB flag is kept in the "0" state.

■ Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I²C control register (address 00DA₁₆) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/W bit) of the address data trans-

mitted by the master is "1." When the ALS bit is "0" and the $\overline{R/\overline{W}}$ bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication preventing function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

■ Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurrence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

Note: The START condition duplication prevention function disables the occurrence of a START condition, reset of bit counter and SCL output when the following condition is satisfied:

- a START condition is set by another master device.

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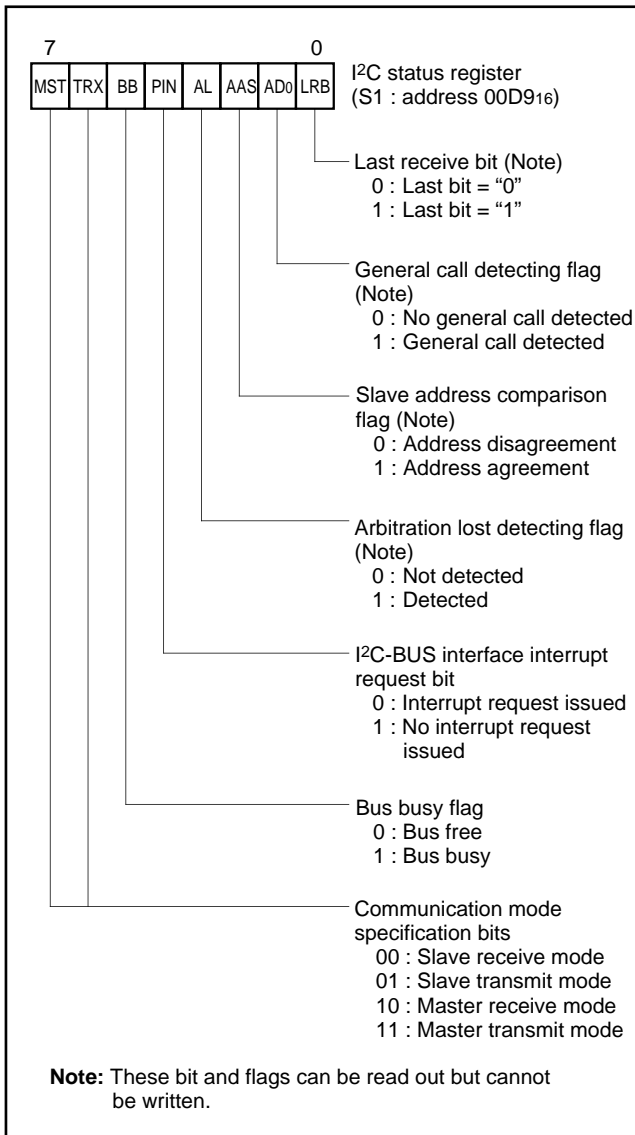


Fig. 19. Structure of I²C status register

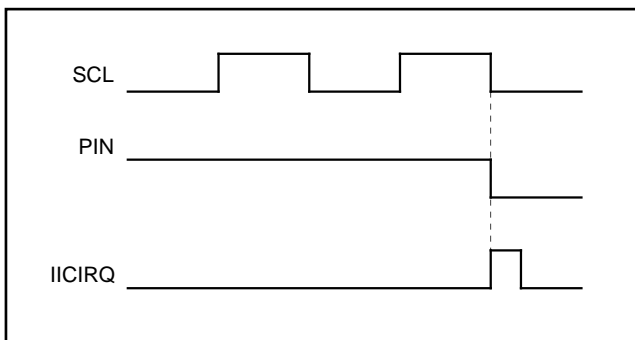


Fig. 20. Interrupt request signal generating timing

(6) START Condition Generating Method

When the ES0 bit of the I²C control register (address 00DA₁₆) is "1," execute a write instruction to the I²C status register (address 00D9₁₆) for setting the MST, TRX and BB bits to "1." Then a START condition occurs. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generating timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 21, the START condition generating timing diagram, and Table 4, the START condition/STOP condition generating timing table.

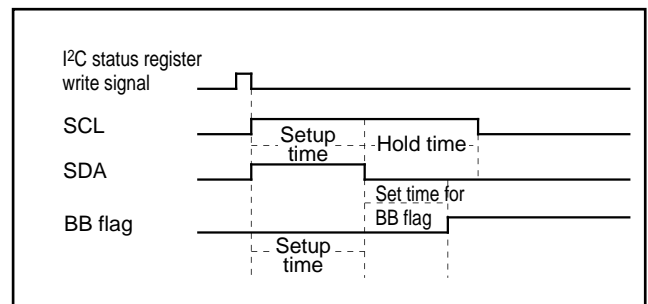


Fig. 21. START condition generating timing diagram

(7) STOP Condition Generating Method

When the ES0 bit of the I²C control register (address 00DA₁₆) is "1," execute a write instruction to the I²C status register (address 00D9₁₆) for setting the MST bit and the TRX bit to "1" and the BB bit to "0." Then a STOP condition occurs. The STOP condition generating timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 22, the STOP condition generating timing diagram, and Table 4, the START condition/STOP condition generating timing table.

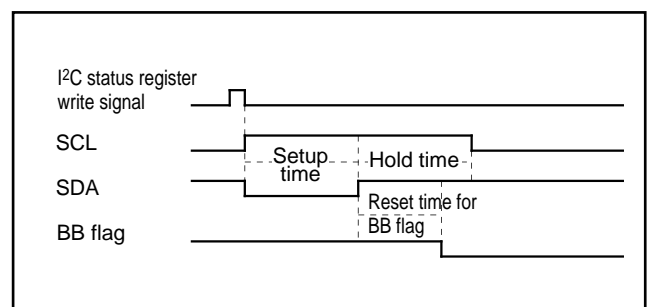


Fig. 22. STOP condition generating timing diagram

Table 4. START condition/STOP condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 μ s (20 cycles)	2.5 μ s (10 cycles)
Hold time	5.0 μ s (20 cycles)	2.5 μ s (10 cycles)
Set/reset time for BB flag	3.0 μ s (12 cycles)	1.5 μ s (6 cycles)

Note: Absolute time at $\phi = 4$ MHz. The value in parentheses denotes the number of ϕ cycles.

(8) START/STOP Condition Detecting Conditions

The START/STOP condition detecting conditions are shown in Figure 23 and Table 5. Only when the 3 conditions of Table 5 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" occurs to the CPU.

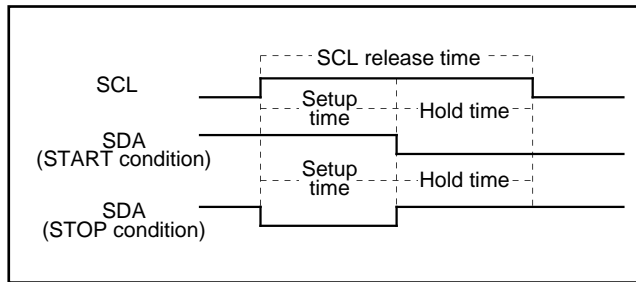


Fig. 23. START condition/STOP condition detecting timing diagram

Table 5. START condition/STOP condition detecting conditions

Standard clock mode	High-speed clock mode
6.5μs (26 cycles) < SCL release time	1.0μs (4 cycles) < SCL release time
3.25μs (13 cycles) < Setup time	0.5μs (2 cycles) < Setup time
3.25μs (13 cycles) < Hold time	0.5μs (2 cycles) < Hold time

Note: Absolute time at $\phi = 4$ MHz. The value in parentheses denotes the number of ϕ cycles.

(9) Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

① 7-bit addressing format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00DA16) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 00D816). At the time of this comparison, address comparison of the RBW bit of the I²C address register (address 00D816) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 24, (1) and (2).

② 10-bit addressing format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00DA16) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I²C address register (address 00D816). At the time of this comparison, an address comparison between the RBW bit of the I²C address register (address 00D816) and the R/W bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/W bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

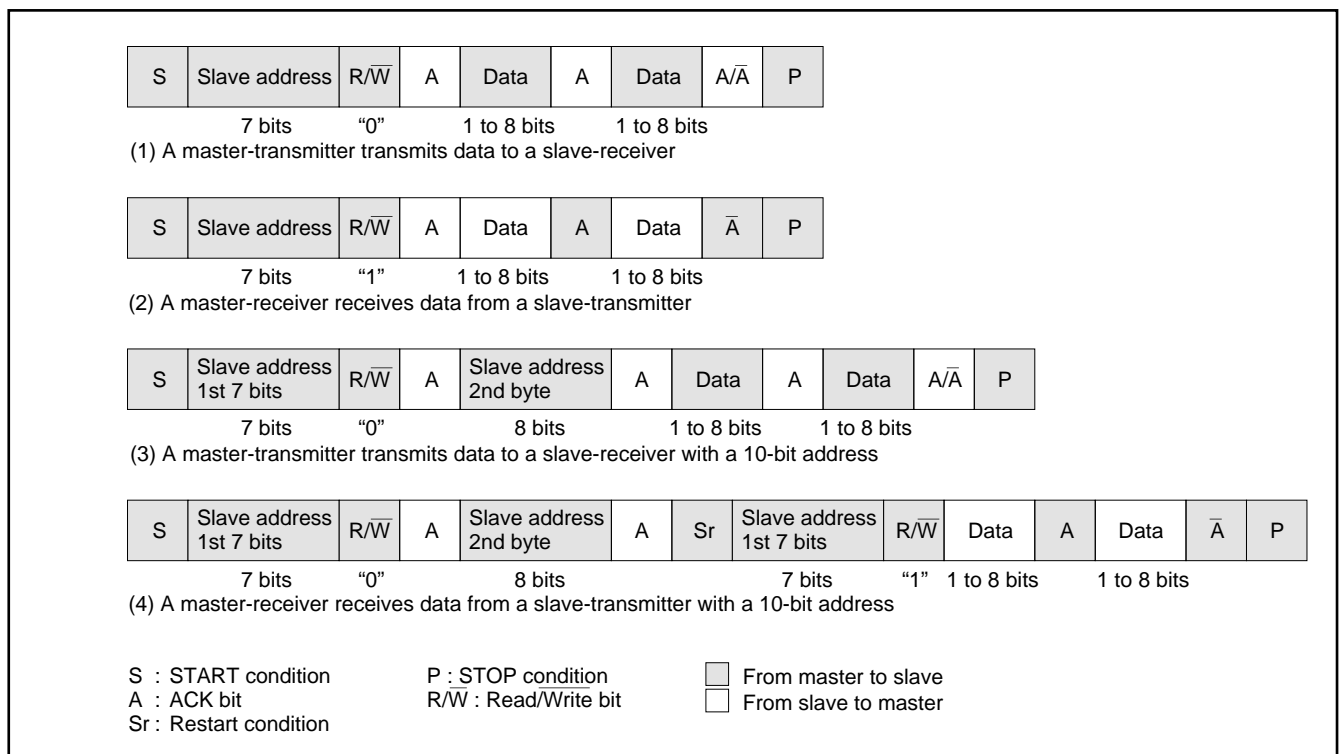


Fig. 24. Address data communication format

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When the first-byte address data matches the slave address, the AAS bit of the I²C status register (address 00D9₁₆) is set to "1." After the second-byte address data is stored into the I²C data shift register (address 00D7₁₆), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd byte matches the slave address, set the RBW bit of the I²C address register (address 00D8₁₆) to "1" by software. This processing can match the 7-bit slave address and R/W data, which are received after a RESTART condition is detected, with the value of the I²C address register (address 00D8₁₆). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 24, (3) and (4).

(10) Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C address register (address 00D8₁₆) and "0" in the RBW bit.
- ② Set the ACK return mode and SCL = 100 kHz by setting "85₁₆" in the I²C clock control register (address 00DB₁₆).
- ③ Set "10₁₆" in the I²C status register (address 00D9₁₆) and hold the SCL at the "H" level.
- ④ Set a communication enable status by setting "48₁₆" in the I²C control register (address 00DA₁₆).
- ⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I²C data shift register (address 00D7₁₆) and set "0" in the least significant bit.
- ⑥ Set "F0₁₆" in the I²C status register (address 00D9₁₆) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
- ⑦ Set transmit data in the I²C data shift register (address 00D7₁₆). At this time, an SCL and an ACK clock automatically occurs.
- ⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
- ⑨ Set "D0₁₆" in the I²C status register (address 00D9₁₆). After this, if ACK is not returned or transmission ends, a STOP condition occurs.

- ⑥ •When all transmitted addresses are "0" (general call)
AD0 of the I²C status register (address 00D9₁₆) is set to "1" and an interrupt request signal occurs.
- When the transmitted addresses match the address set in ①
AAS of the I²C status register (address 00D9₁₆) is set to "1" and an interrupt request signal occurs.
- In the cases other than the above
AD0 and AAS of the I²C status register (address 00D9₁₆) are set to "0" and no interrupt request signal occurs.
- ⑦ Set dummy data in the I²C data shift register (address 00D7₁₆).
- ⑧ When receiving control data of more than 1 byte, repeat step ⑦.
- ⑨ When a STOP condition is detected, the communication ends.

(11) Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C address register (address 00D8₁₆) and "0" in the RBW bit.
- ② Set the no ACK clock mode and SCL = 400 kHz by setting "25₁₆" in the I²C clock control register (address 00DB₁₆).
- ③ Set "10₁₆" in the I²C status register (address 00D9₁₆) and hold the SCL at the "H" level.
- ④ Set a communication enable status by setting "48₁₆" in the I²C control register (address 00DA₁₆).
- ⑤ When a START condition is received, an address comparison is made.

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PWM OUTPUT FUNCTION

The M37221EF-XXXSP is equipped with a 14-bit PWM (DA) and six 8-bit PWMs (PWM0–PWM5). DA has a 14-bit resolution with the minimum resolution bit width of $0.25\mu\text{s}$ (for $f(X_{IN}) = 8\text{ MHz}$) and a repeat period of $4096\mu\text{s}$. PWM0–PWM5 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of $4\mu\text{s}$ (for $f(X_{IN}) = 8\text{ MHz}$) and repeat period of $1024\mu\text{s}$.

Figure 25 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM5 using $f(X_{IN})$ divided by 2 as a reference signal.

(1) Data Setting

When outputting DA, first set the high-order 8 bits to the DA-H register (address $00CE_{16}$), then the low-order 6 bits to the DA-L register (address $00CF_{16}$). When outputting PWM0–PWM5, set 8-bit output data in the PWMi register (i means 0 to 5; addresses $00D0_{16}$ to $00D4_{16}$, $00F6_{16}$).

(2) Transmitting Data from Register to PWM circuit

Data transfer from the 8-bit PWM register to 8-bit PWM circuit is executed at writing data to the register.

The signal output from the 8-bit PWM output pin corresponds to the contents of this register.

Also, data transfer from the DA register (addresses $00CE_{16}$ and $00CF_{16}$) to the 14-bit PWM circuit is executed at writing data to the DA-L register (address $00CF_{16}$). Reading from the DA-H register (address $00CE_{16}$) means reading this transferred data. Accordingly, it is possible to confirm the data being output from the D-A output pin by reading the DA register.

(3) Operating of 8-bit PWM

The following is the explanation about PWM operation.

At first, set the bit 0 of PWM output control register 1 (address $00D5_{16}$) to "0" (at reset, this bit 0 already set to "0" automatically), so that the PWM count source is supplied.

PWM0–PWM5 are also used as pins P00–P05 respectively. For PWM0–PWM5, set the corresponding bits of the port P0 direction register to "1" (output mode). And select each output polarity by bit 3 of the PWM output control register 2 (address $00D6_{16}$). Then, set bits 2 to 7 of the PWM output control register 1 to "1" (PWM output). The PWM waveform is output from the PWM output pins by setting these registers.

Figure 26 shows the 8-bit PWM timing. One cycle (T) is composed of $256 (2^8)$ segments. The 8 kinds of pulses relative to the weight of each bit (bits 0 to 7) are output inside the circuit during 1 cycle. Refer to Figure 26 (a). The 8-bit PWM outputs waveform performed a OR operation of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 26 (b). 256 kinds of output ("H" level area: $0/256$ to $255/256$) are selected by changing the contents of the PWM register. A length of entirely "H" output cannot be output, i.e. $256/256$.

(4) Operating of 14-bit PWM

As with 8-bit PWM, set the bit 0 of the PWM output control register 1 (address $00D5_{16}$) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied. Next, select the output polarity by bit 2 of the PWM output control register 2 (address $00D6_{16}$). Then, the 14-bit PWM outputs from the D-A output pin by setting bit 1 of the PWM output control register 1 to "0" (at reset, this bit already set to "0" automatically) to select the DA output.

The output example of the 14-bit PWM is shown in Figure 27.

The 14-bit PWM divides the data of the DA latch into the low-order 6 bits and the high-order 8 bits.

The fundamental waveform is determined with the high-order 8-bit data "DH." A "H" level area with a length $\tau \times D_H$ ("H" level area of fundamental waveform) is output every short area of " t " = $256\tau = 64\mu\text{s}$ (τ is the minimum resolution bit width of $0.25\mu\text{s}$). The "H" level area increase interval (t_m) is determined with the low-order 6-bit data "DL." The "H" level area of smaller intervals " t_m " shown in Table 6 is longer by τ than that of other smaller intervals in PWM repeat period " T " = $64t$. Thus, a rectangular waveform with the different "H" width is output from the D-A pin. Accordingly, the PWM output changes by τ unit pulse width by changing the contents of the DA-H and DA-L registers. A length of entirely "H" output cannot be output, i. e. $256/256$.

(5) Output after Reset

At reset the output of port P00–P05 is in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

Table 6. Relation between the low-order 6-bit data and high-level area increase interval

Low-order 6 bits of data	Area longer by τ than that of other t_m ($m = 0$ to 63)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m = 32$
0 0 0 0 1 0	$m = 16, 48$
0 0 0 1 0 0	$m = 8, 24, 40, 56$
0 0 1 0 0 0	$m = 4, 12, 20, 28, 36, 44, 52, 60$
0 1 0 0 0 0	$m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m = 1, 3, 5, 7, \dots, 57, 59, 61, 63$

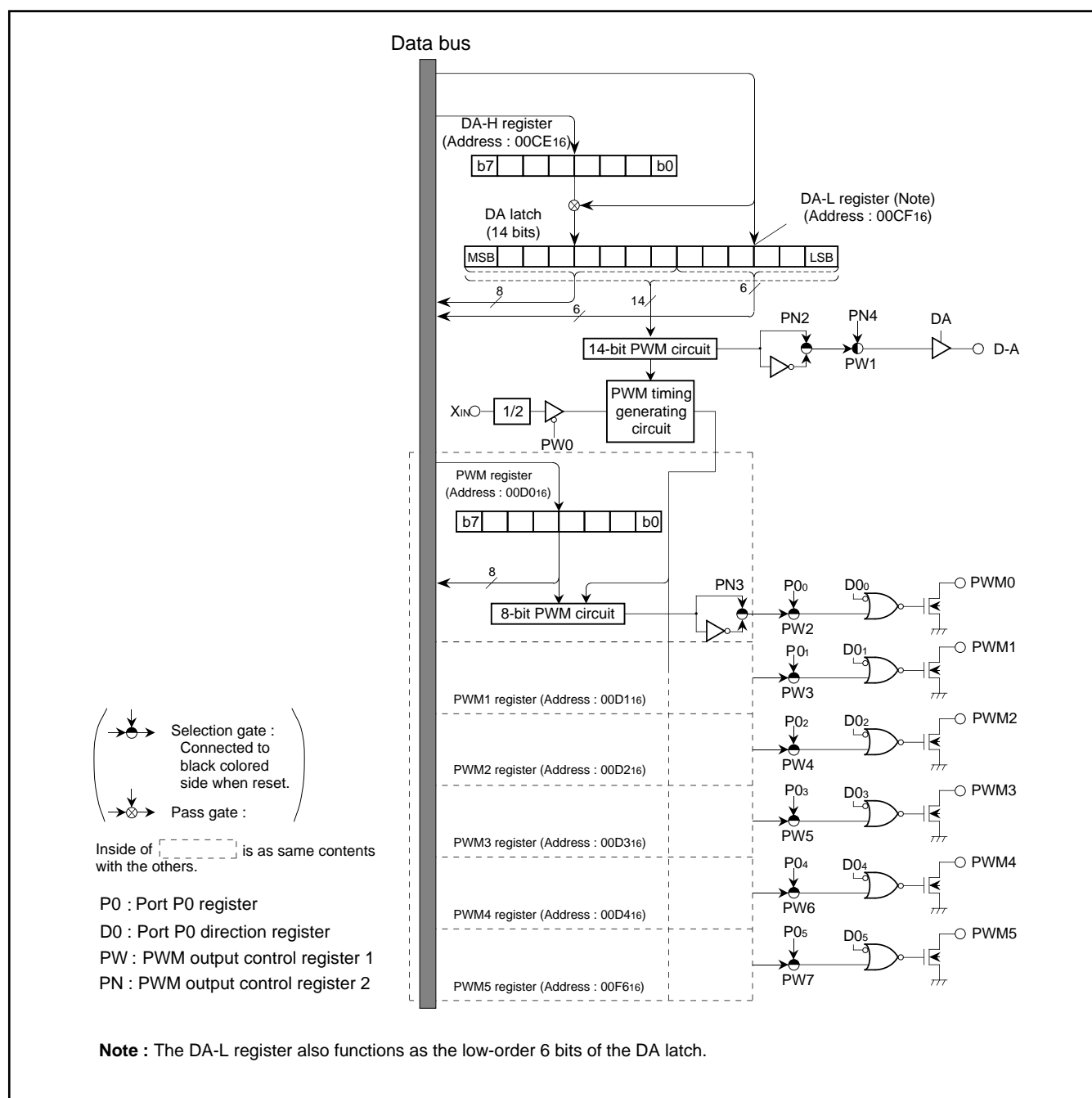


Fig. 25. PWM block diagram

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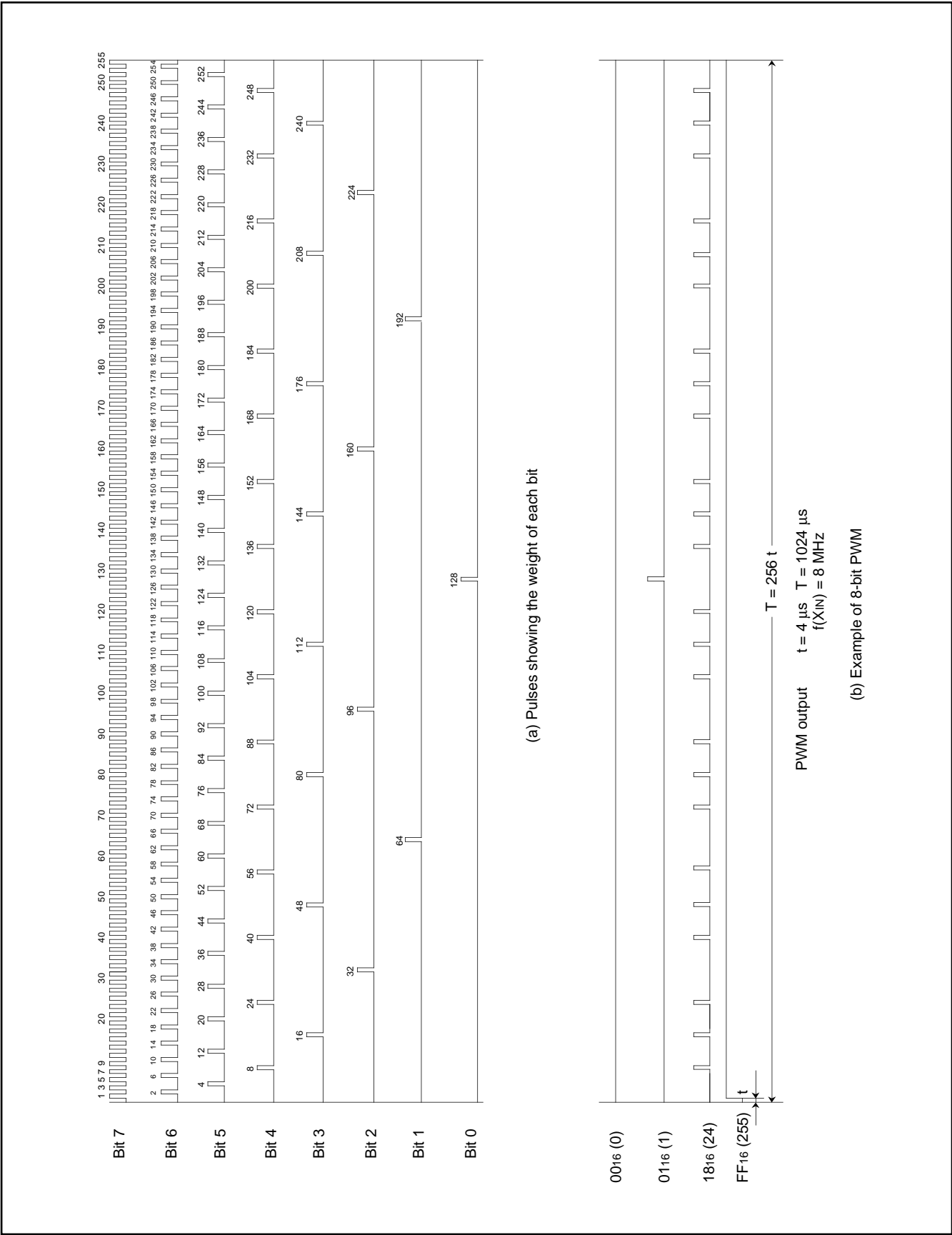


Fig. 26. 8-bit PWM timing

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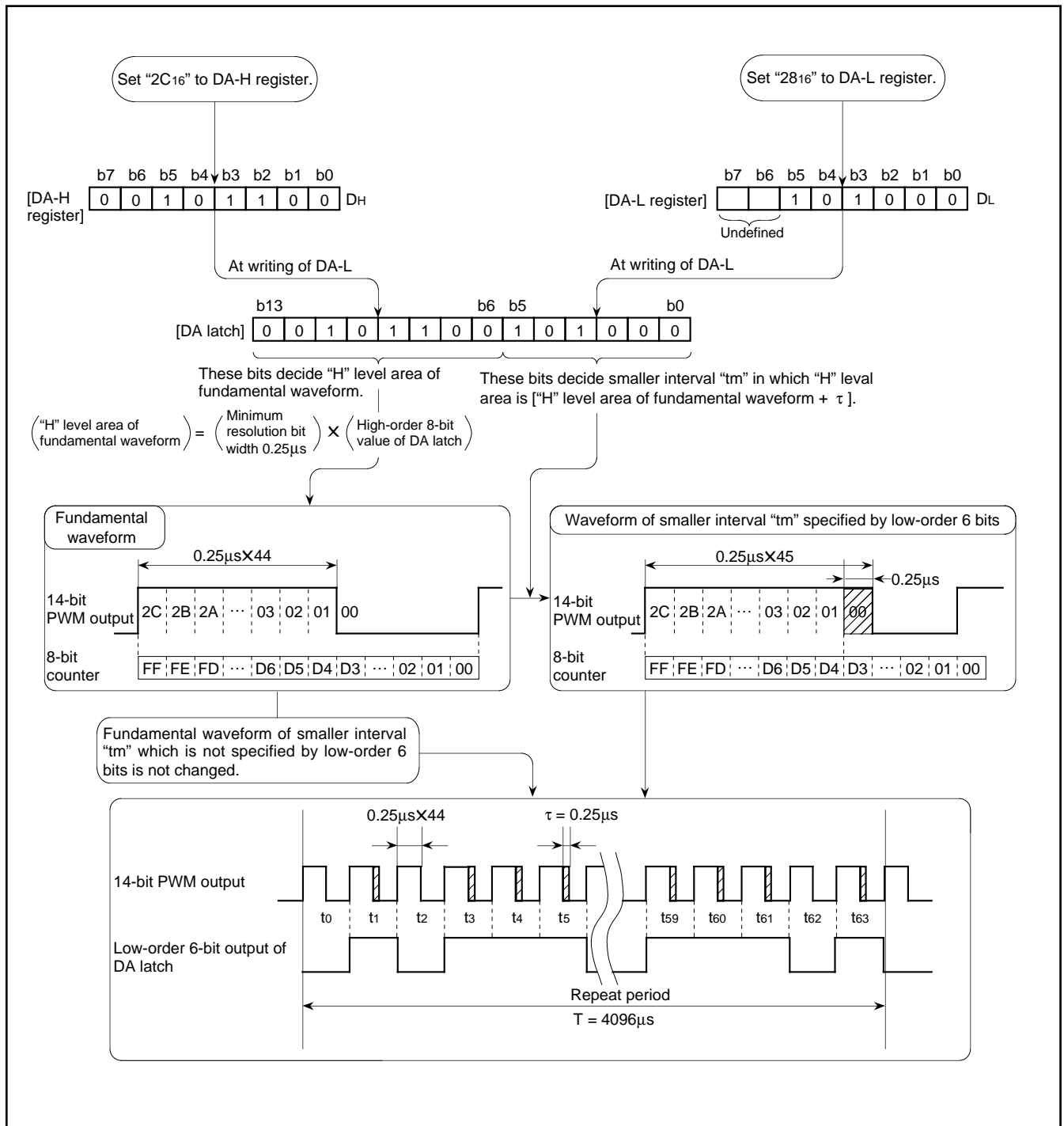


Fig. 27. 14-bit PWM output example ($f(X_{IN}) = 8 \text{ MHz}$)

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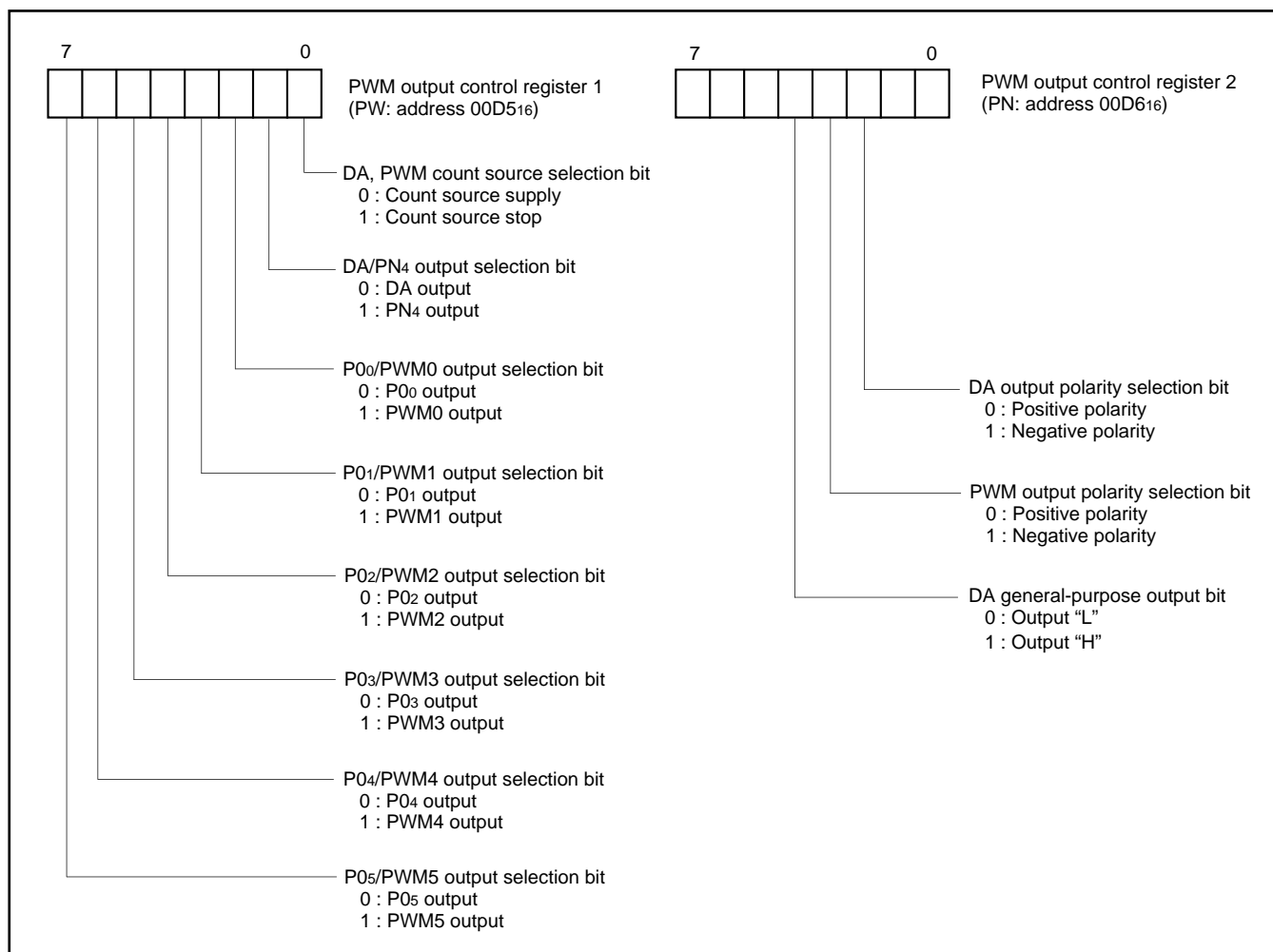


Fig. 28. Structure of PWM-related registers

A-D COMPARATOR

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 31.

The reference voltage "V_{ref}" for D-A conversion is set by bits 0 to 5 of the A-D control register 2 (address 00EF₁₆).

The comparison result of the analog input voltage and the reference voltage "V_{ref}" is stored in bit 4 of the A-D control register 1 (address 00EE₁₆).

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the data for select of analog input pins to bits 0 to 2 of the A-D control register 1 and write the digital value corresponding to V_{ref} to be compared to the bits 0 to 5 of the A-D control register 2. The voltage comparison starts by writing to the A-D control register 2, and it is completed after 16 machine cycles (NOP instruction X 8).

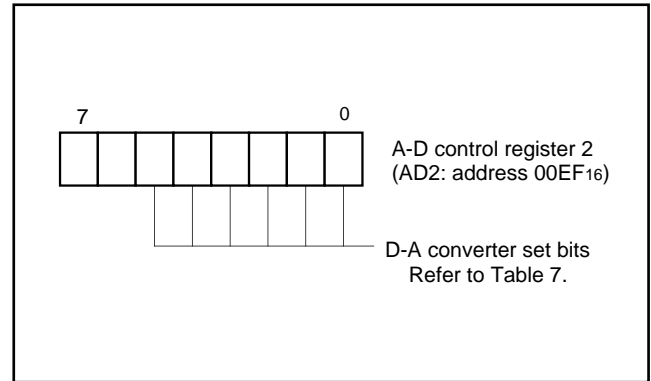


Fig.30. Structure of A-D control register 2

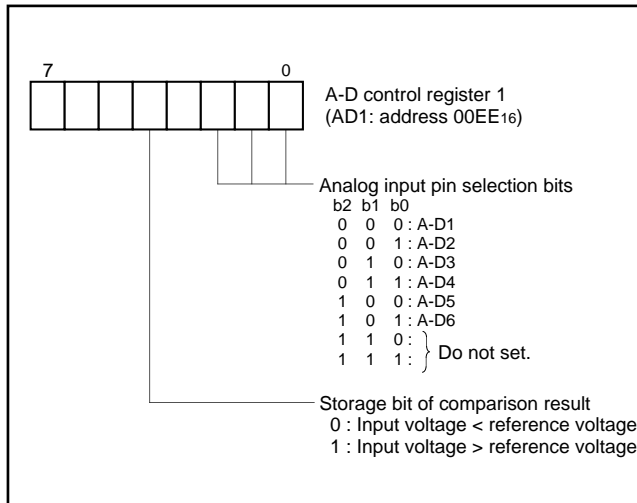


Fig. 29. Structure of A-D control register 1

Table 7. Relation between contents of A-D control register 2 and reference voltage "V_{ref}"

A-D control register 2						Reference voltage "V _{ref} "
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	1/128 V _{CC}
0	0	0	0	0	1	3/128 V _{CC}
0	0	0	0	1	0	5/128 V _{CC}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	123/128 V _{CC}
1	1	1	1	1	0	125/128 V _{CC}
1	1	1	1	1	1	127/128 V _{CC}

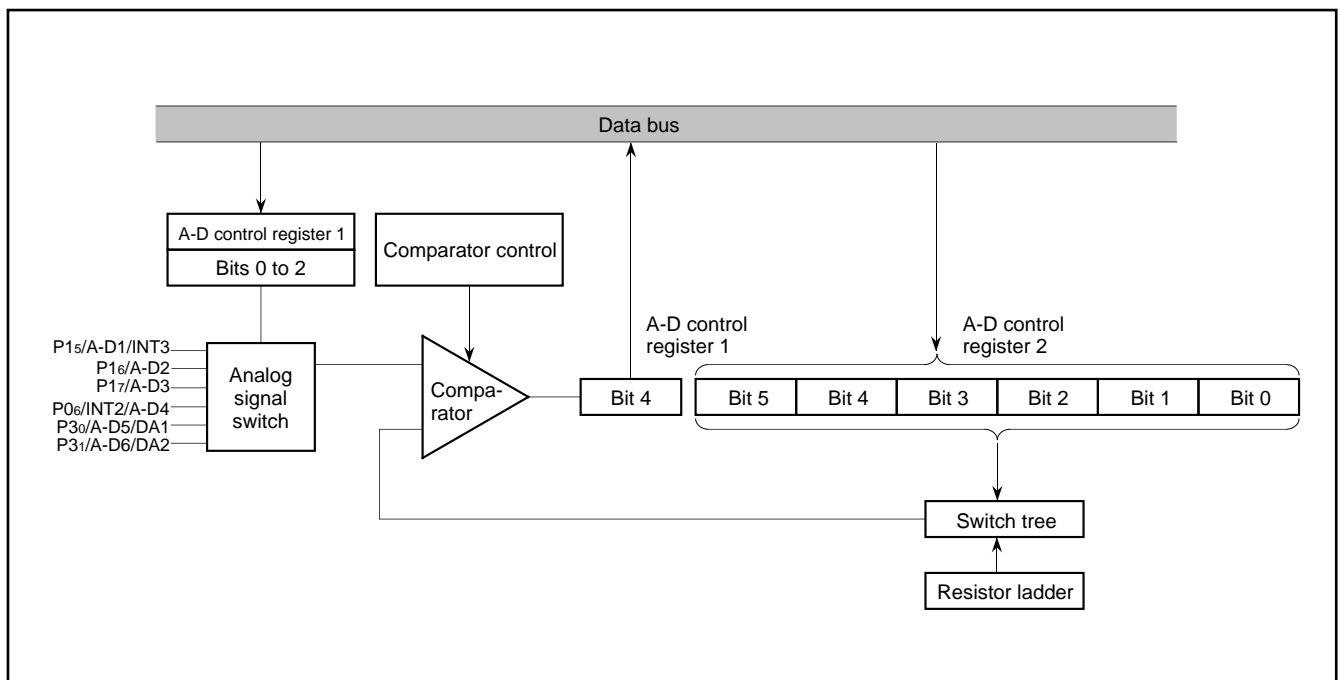


Fig. 31. A-D comparator block diagram

D-A CONVERTER

The M37221EF-XXXSP has 2 D-A converters with 6-bit resolution. D-A converter block diagram is shown in Figure 34.

D-A conversion is performed by setting the value in the DA conversion register. The result of D-A conversion is output from the DA pin by setting "1" to the DA output enable bit of the port P3 output mode control register (bits 2 and 3 at address 00CD₁₆).

The output analog voltage V is determined with the value n (n: decimal number) in the DA conversion register.

$$V = V_{CC} \times \frac{n}{64} \quad (n = 0 \text{ to } 63)$$

The DA output does not build in a buffer, so connect an external buffer when driving a low-impedance load.

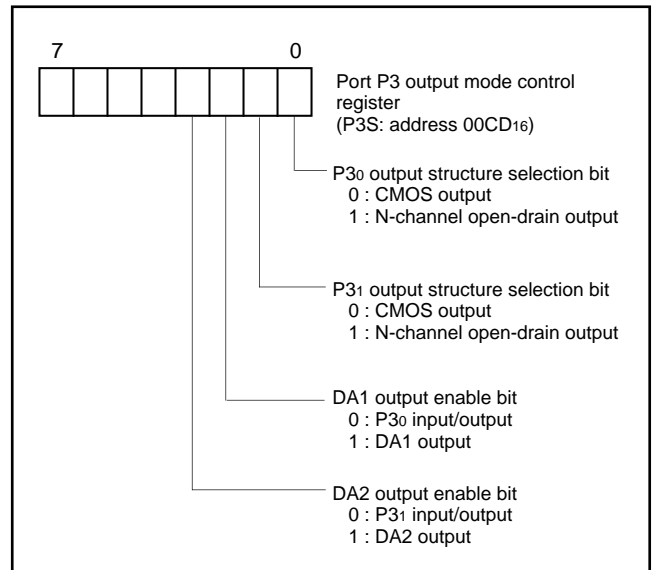


Fig. 33. Structure of port P3 output mode register

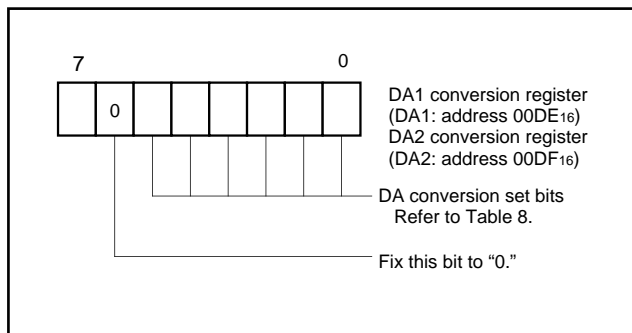


Fig. 32. Structure of D-A converter register

Table 8. Relation between contents of D-A conversion register and output voltage

D-A conversion register						Output voltage "V"
Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	0	0/64 V _{CC}
0	0	0	0	0	1	1/64 V _{CC}
0	0	0	0	1	0	2/64 V _{CC}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	1	61/64 V _{CC}
1	1	1	1	1	0	62/64 V _{CC}
1	1	1	1	1	1	63/64 V _{CC}

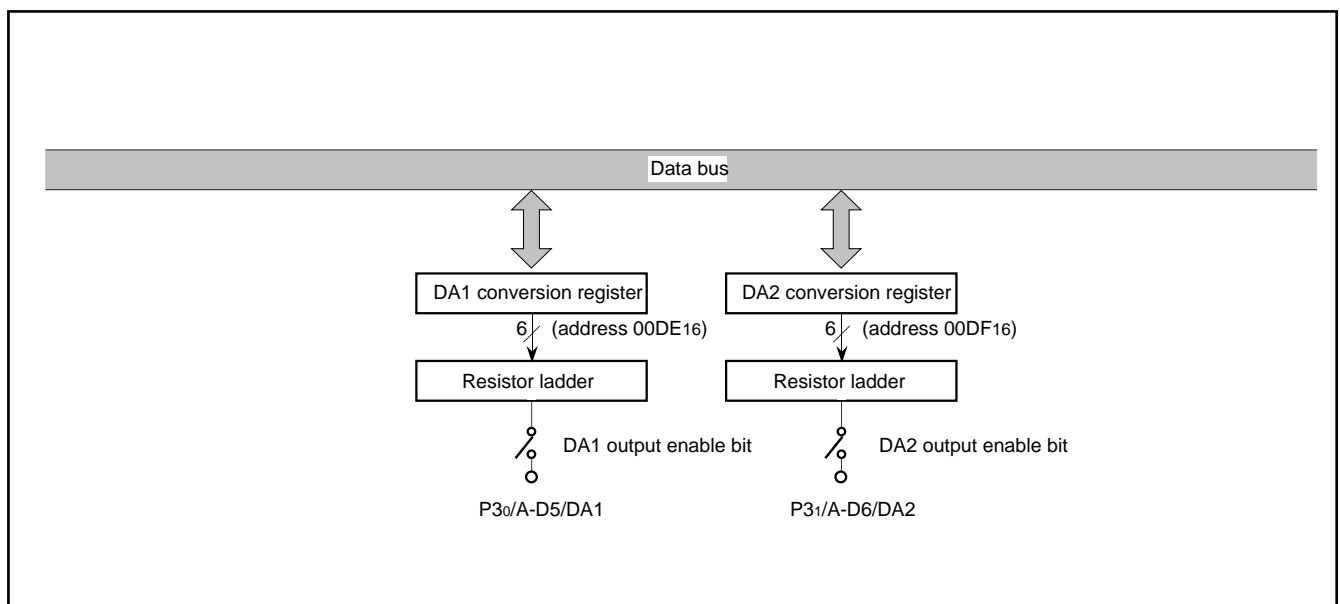


Fig. 34. D-A converter block diagram

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 9 outlines the CRT display functions of the M37221EF-XXXSP. The M37221EF-XXXSP incorporates a CRT display control circuit of 24 characters X 2 lines. CRT display is controlled by the CRT control register. Up to 256 kinds of characters can be displayed. The colors can be specified for each character and up to 4 kinds of colors can be displayed on one screen. A combination of up to 7 colors can be obtained by using each output signal (R, G, and B).

Characters are displayed in a 12 X 16 dots configuration to obtain smooth character patterns (refer to Figure 35).

The following shows the procedure how to display characters on the CRT screen.

- ① Write the display character code in the display RAM.
- ② Specify the display color by using the color register.
- ③ Write the color register in which the display color is set in the display RAM.
- ④ Specify the vertical position by using the vertical position register.
- ⑤ Specify the character size by using the character size register.
- ⑥ Specify the horizontal position by using the horizontal position register.
- ⑦ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT display starts according to the input of the VSYNC signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (3 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 36 shows the structure of the CRT display control register.

Figure 37 shows the block diagram of the CRT display control circuit.

Table 9. Outline of CRT display functions

Parameter		Functions
Number of display characters		24 characters X 2 lines
Dot structure		12 X 16 dots (refer to Figure 35)
Kinds of characters		256 kinds
Kinds of character sizes		3 kinds
Color	Kinds of colors	1 screen: 4 kinds, maximum 7 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 7 kinds)
Character background coloring		Possible (a character unit, 1 screen : 4 kinds, maximum 7 kinds)

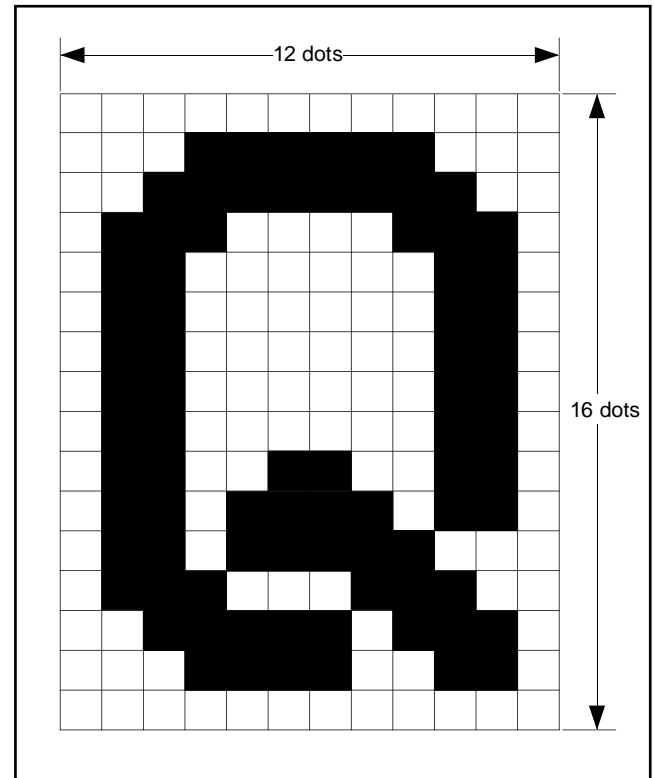


Fig. 35. CRT display character configuration

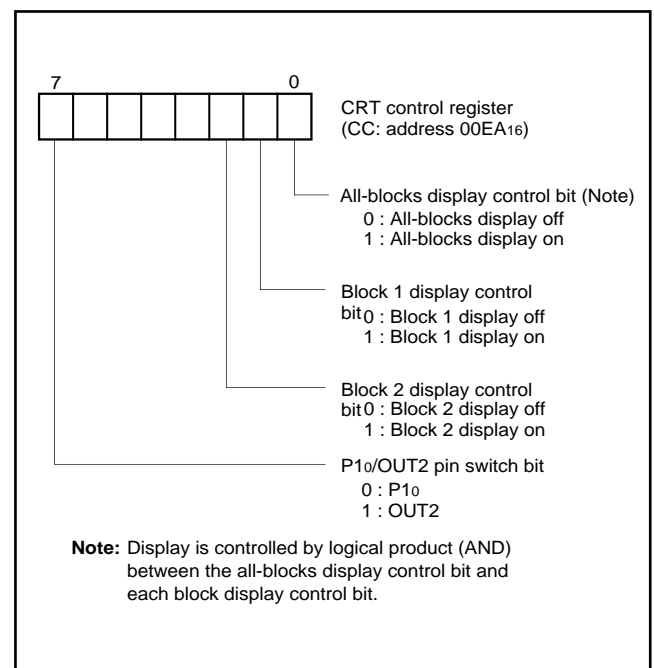


Fig. 36. Structure of CRT control register

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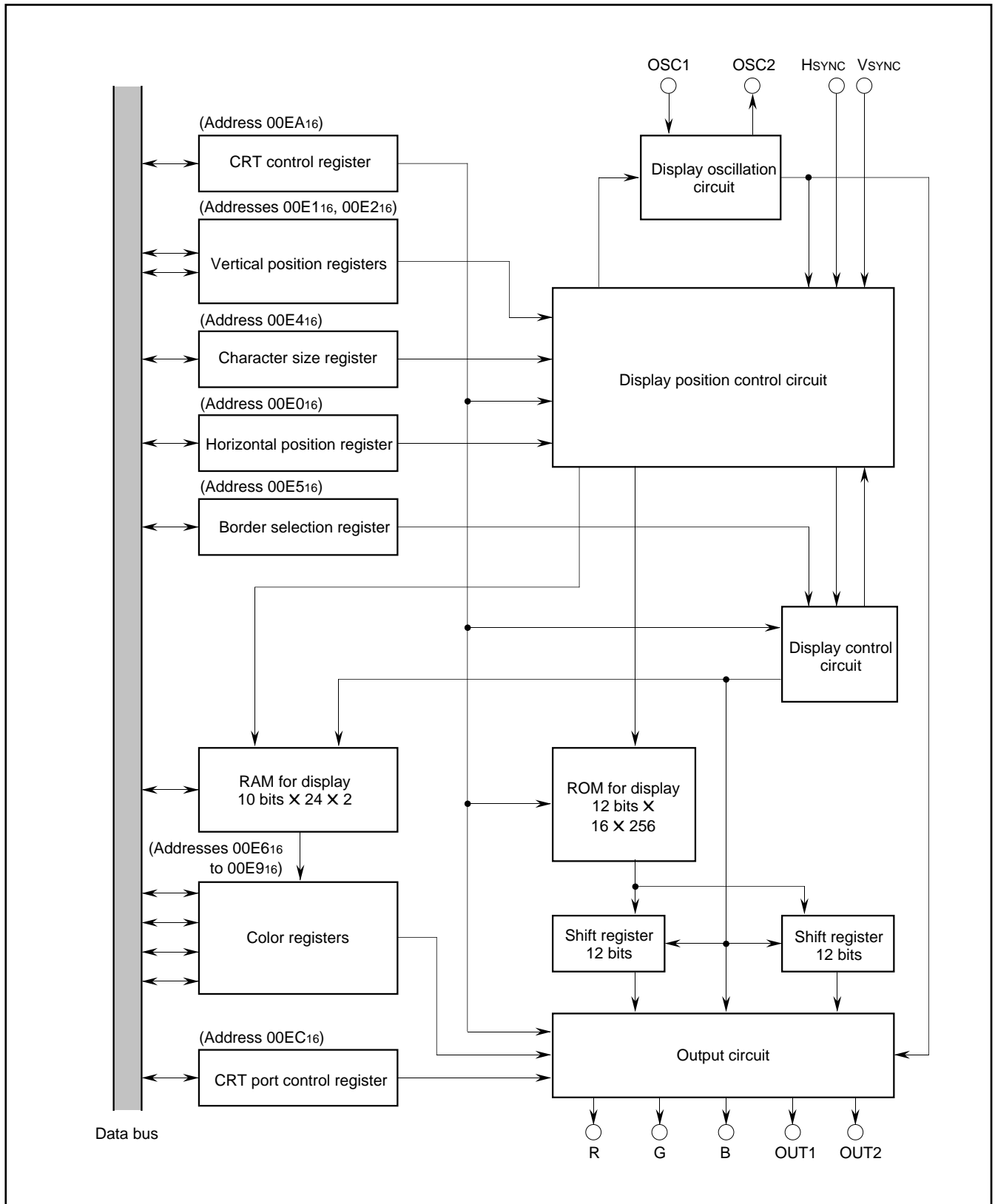


Fig. 37. Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are 2 blocks, block 1 and block 2. Up to 20 characters can be displayed in each block (refer to (4) Memory for Display).

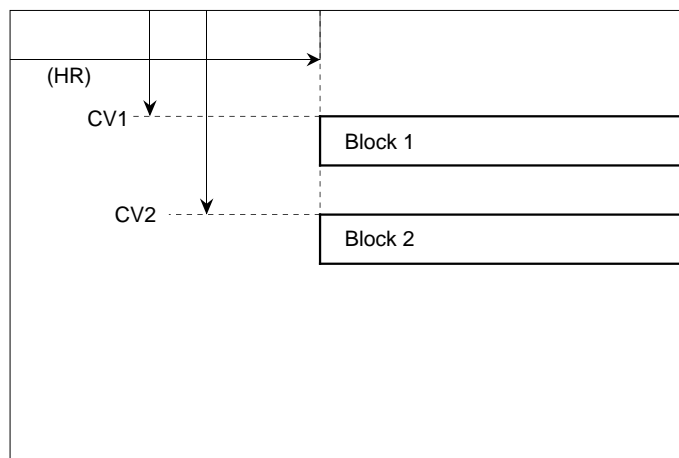
The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 64-step display positions in units of 4Tc (Tc = oscillating cycle for display).

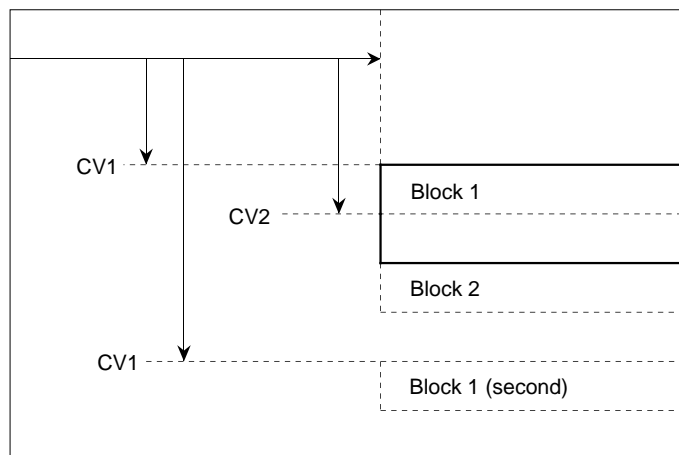
The display position in the vertical direction for each block can be selected from 128-step display positions in units of 4 scanning lines.

Block 2 is displayed after the display of block 1 is completed (refer to Figure 38 (a)). Accordingly, if the display of block 2 starts during the display of block 1, only block 1 is displayed. Similarly, when multiline display, block 1 is displayed after the display of block 2 is completed (refer to Figure 38 (b)).

The vertical position can be specified from 128-step positions (4 scanning lines per a step) for each block by setting values "00₁₆" to "7F₁₆" to bits 0 to 6 in the vertical position register (addresses 00E1₁₆ and 00E2₁₆). Figure 40 shows the structure of the vertical position register.



(a) Example when each block is separated



(b) Example when block 2 overlaps with block 1

← No display

← No display

Fig. 38. Display position

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The display position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time, it starts to count the rising edge (falling edge) of HSYNC signal from after about 1 machine cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the CRT port control register (address 00EC16). For details, refer to (8) CRT Output Pin Control.

Note: When bits 0 and 1 of the CRT port control register (address 00EC16) are set to "1" (negative polarity), the vertical position is determined by counting falling edge of HSYNC signal after rising edge of VSYNC control signal in the microcomputer (refer to Figure 39).

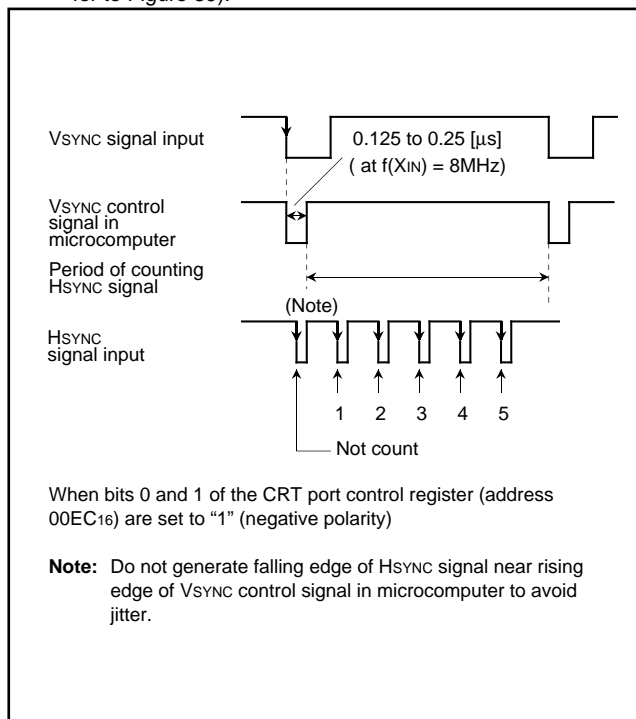


Fig. 39. Supplement explanation for display position

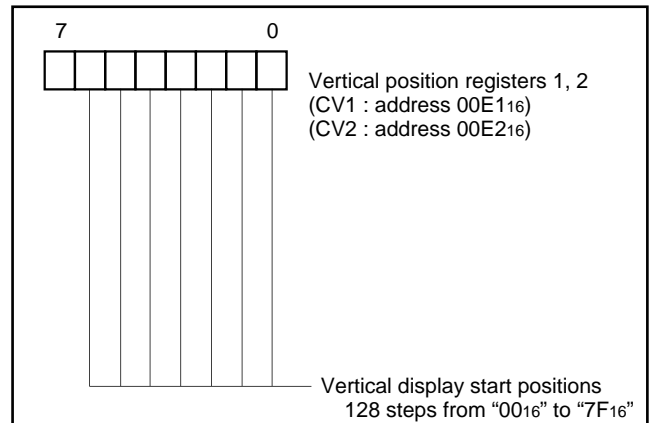


Fig. 40. Structure of vertical position register

The horizontal position is common to all blocks, and can be set in 64 steps (where 1 step is 4Tc, Tc being the display oscillation period) as values "0016" to "3F16" in bits 0 to 5 of the horizontal position register (address 00E016). The structure of the horizontal position register is shown in Figure 41.

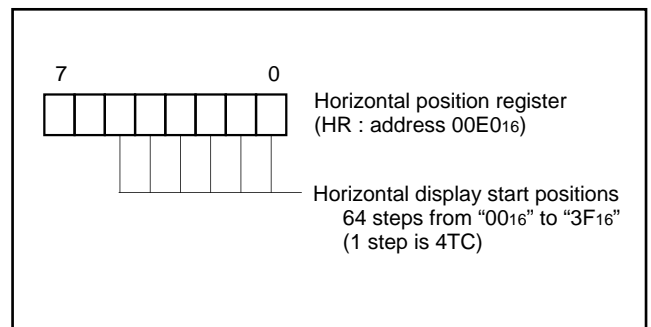


Fig. 41. Structure of horizontal position register

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(3) Character Size

The size of characters to be displayed can be from 3 sizes for each block. Use the character size register (address 00E416) to set a character size. The character size of block 1 can be specified by using bits 0 and 1 of the character size register; the character size of block 2 can be specified by using bits 2 and 3. Figure 42 shows the structure of the character size register.

The character size can be selected from 3 sizes: minimum size, medium size and large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the oscillating cycle for display (T_c) in the width (horizontal) direction. The minimum size consists of [1 scanning line] \times [$1T_c$]; the medium size consists of [2 scanning lines] \times [$2T_c$]; and the large size consists of [3 scanning lines] \times [$3T_c$]. Table 10 shows the relation between the set values in the character size register and the character sizes.

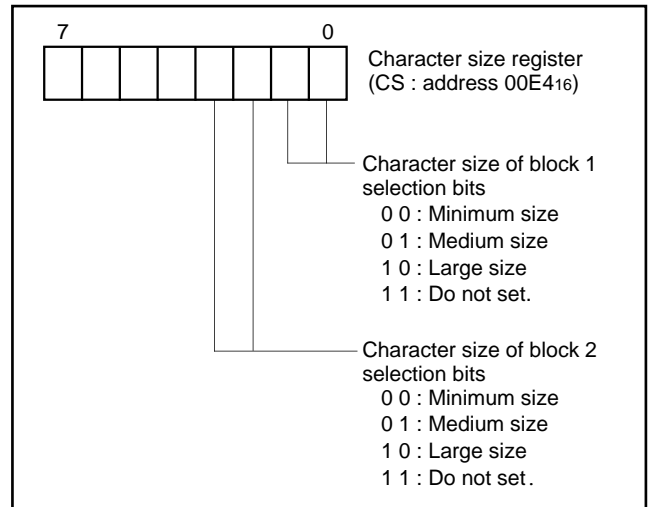


Fig. 42. Structure of character size register

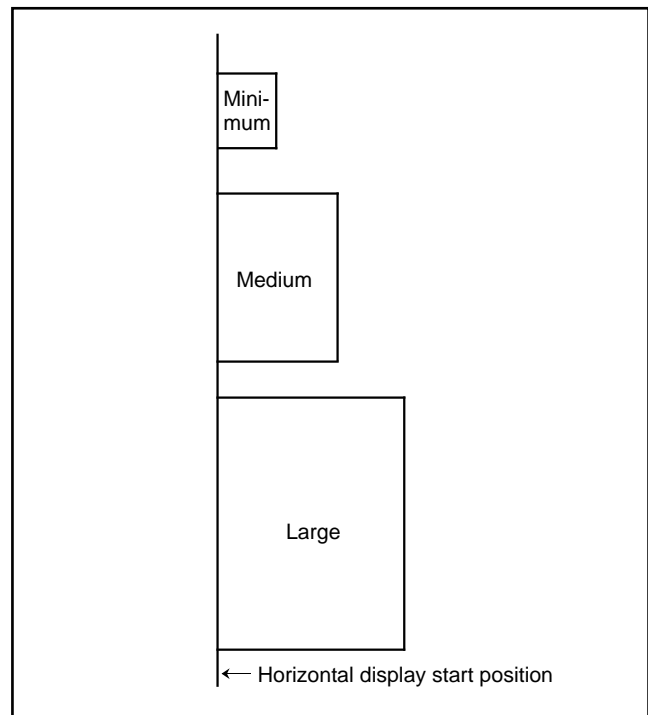


Fig. 43. Display start position of each character size (horizontal direction)

Table 10. Relation between set values in character size register and character sizes

Set values of character size register		Character size	Width (horizontal) direction T_c : oscillating cycle for display	Height (vertical) direction scanning lines
CSn1	CSn0			
0	0	Minimum	$1T_c$	1
0	1	Medium	$2T_c$	2
1	0	Large	$3T_c$	3
1	1	This is not available		

Note: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 43).

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(4) Memory for Display

There are 2 types of display memory : CRT display ROM (addresses 10000₁₆ to 11FFF₁₆) used to store character dot data (masked) and CRT display RAM (addresses 0600₁₆ to 06B7₁₆) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for display (addresses 10000₁₆ to 11FFF₁₆)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM. The character code list is shown in Table 11.

The CRT display ROM has a capacity of 8 K bytes. Since 32 bytes are required for 1 character data, the ROM can store up to 256 kinds of characters.

The CRT display ROM space is broadly divided into 2 areas. The [vertical 16 dots] X [horizontal (left side) 8 dots] data of display characters are stored in addresses 10000₁₆ to 107FF₁₆ and 11000₁₆ to 117FF₁₆; the [vertical 16 dots] X [horizontal (right side) 4 dots] data of display characters are stored in addresses 10800₁₆ to 10FFF₁₆ and 11800₁₆ to 11FFF₁₆ (refer to Figure 44). Note however that the high-order 4 bits in the data to be written to addresses 10800₁₆ to 10FFF₁₆ and 11800₁₆ to 11FFF₁₆ must be set to "1" (by writing data "FX₁₆").

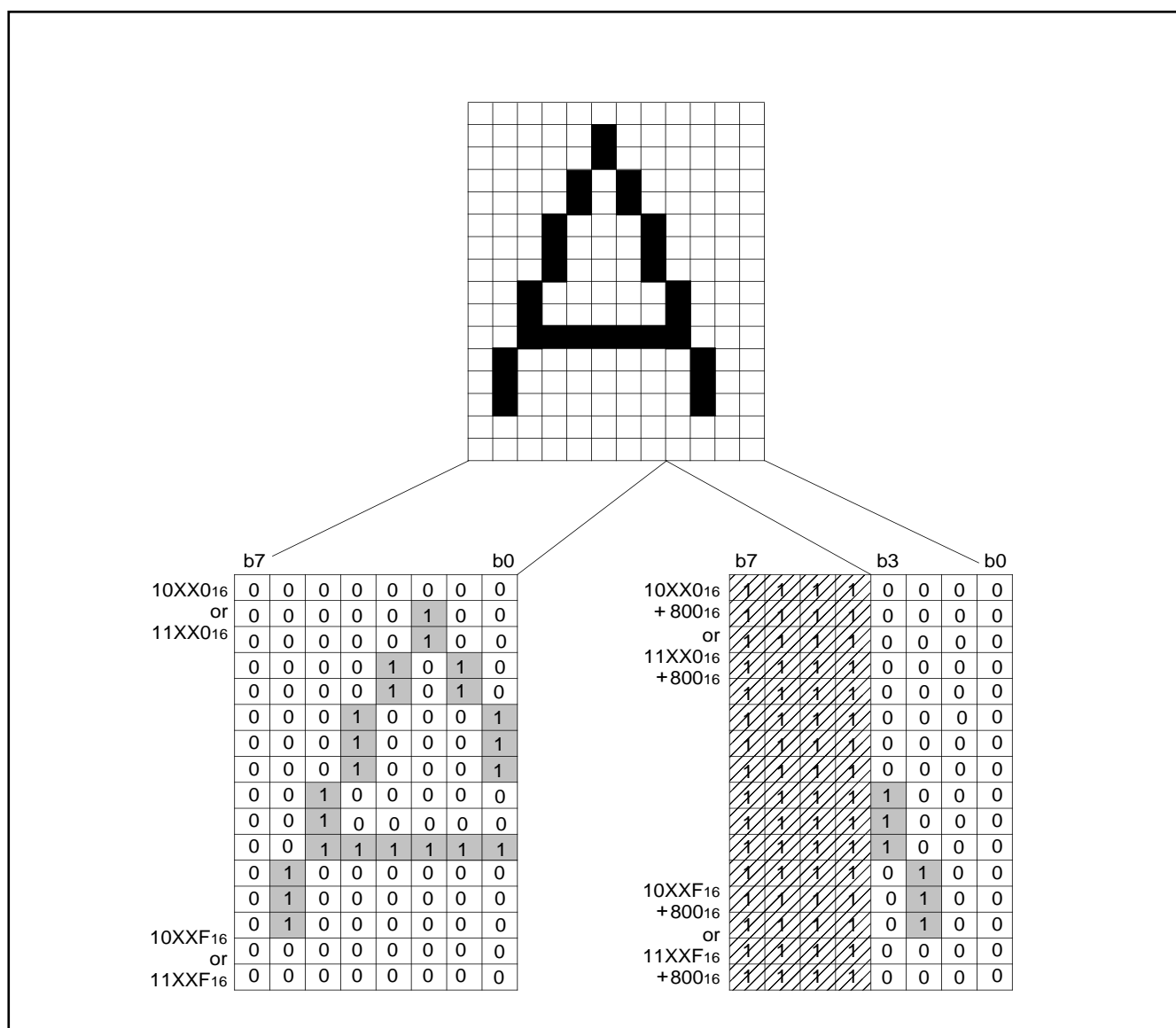


Fig. 44. Display character stored data

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Table 11. Character code list (partially abbreviated)

Character code	Character data storage address	
	Left 8 dots lines	Right 4 dots lines
00 ₁₆	1000 ₁₆ to 100F ₁₆	1080 ₁₆ to 108F ₁₆
01 ₁₆	1001 ₁₆ to 100F ₁₆	1081 ₁₆ to 108F ₁₆
02 ₁₆	1002 ₁₆ to 100F ₁₆	1082 ₁₆ to 108F ₁₆
03 ₁₆	1003 ₁₆ to 100F ₁₆	1083 ₁₆ to 108F ₁₆
:	:	:
7E ₁₆	107E ₁₆ to 107F ₁₆	10FE ₁₆ to 10FF ₁₆
7F ₁₆	107F ₁₆ to 107F ₁₆	10FF ₁₆ to 10FF ₁₆
80 ₁₆	1100 ₁₆ to 110F ₁₆	1180 ₁₆ to 118F ₁₆
81 ₁₆	1101 ₁₆ to 110F ₁₆	1181 ₁₆ to 118F ₁₆
:	:	:
FD ₁₆	117D ₁₆ to 117F ₁₆	11FD ₁₆ to 11FF ₁₆
FE ₁₆	117E ₁₆ to 117F ₁₆	11FE ₁₆ to 11FF ₁₆
FF ₁₆	117F ₁₆ to 117F ₁₆	11FF ₁₆ to 11FF ₁₆

② RAM for display (addresses 0600₁₆ to 06B7₁₆)

The CRT display RAM is allocated at addresses 0600₁₆ to 06B7₁₆, and is divided into a display character code specification part and display color specification part for each block. Table 12 shows the contents of the CRT display RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address 0600₁₆ and write the color register No. to the low-order 2 bits (bits 0 and 1) in address 0680₁₆. The color register No. to be written here is one of the 4 color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers. The structure of the CRT display RAM is shown in Figure 45.

Table 12. Contents of CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st character	0600 ₁₆	0680 ₁₆
	2nd character	0601 ₁₆	0681 ₁₆
	3rd character	0602 ₁₆	0682 ₁₆
	:	:	:
	22nd character	0615 ₁₆	0695 ₁₆
	23rd character	0616 ₁₆	0696 ₁₆
	24th character	0617 ₁₆	0697 ₁₆
Not used		0618 ₁₆ to 061F ₁₆	0698 ₁₆ to 069F ₁₆
Block 2	1st character	0620 ₁₆	06A0 ₁₆
	2nd character	0621 ₁₆	06A1 ₁₆
	3rd character	0622 ₁₆	06A2 ₁₆
	:	:	:
	22nd character	0635 ₁₆	06B5 ₁₆
	23rd character	0636 ₁₆	06B6 ₁₆
	24th character	0637 ₁₆	06B7 ₁₆

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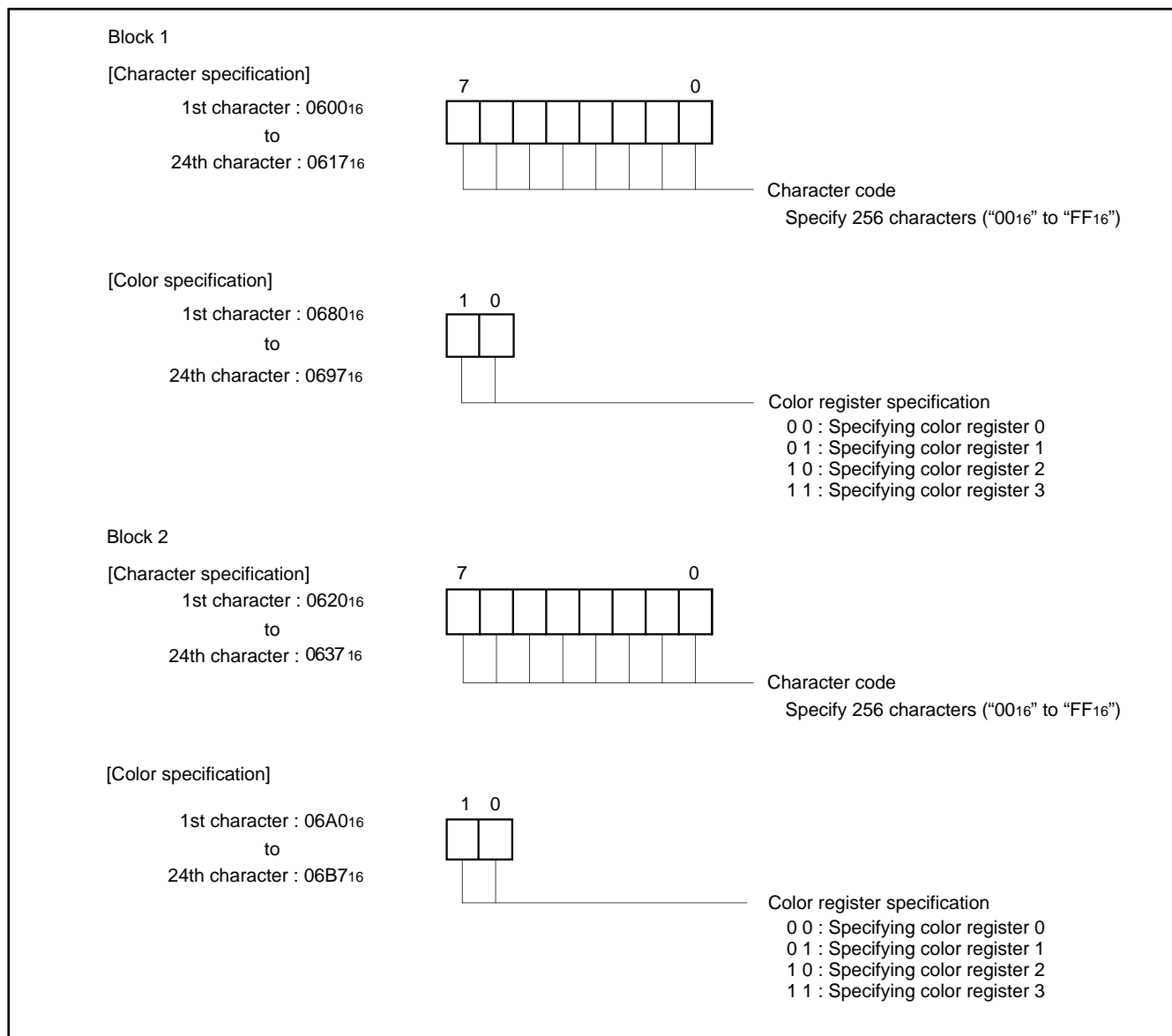


Fig. 45. Structure of CRT display RAM

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(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the 4 registers (CO0 to CO3: addresses 00E616 to 00E916) and then specifying that color register with the CRT display RAM. There are 3 color outputs; R, G and B. By using a combination of these outputs, it is possible to set 2^3-1 (when no output) = 7 colors. However, since only 4 color registers are available, up to 4 colors can be disabled at one time.

R, G and B outputs are set by using bits 1 to 3 in the color register. Bit 5 is used to specify whether a character output or blank output. Figure 46 shows the structure of the color register.

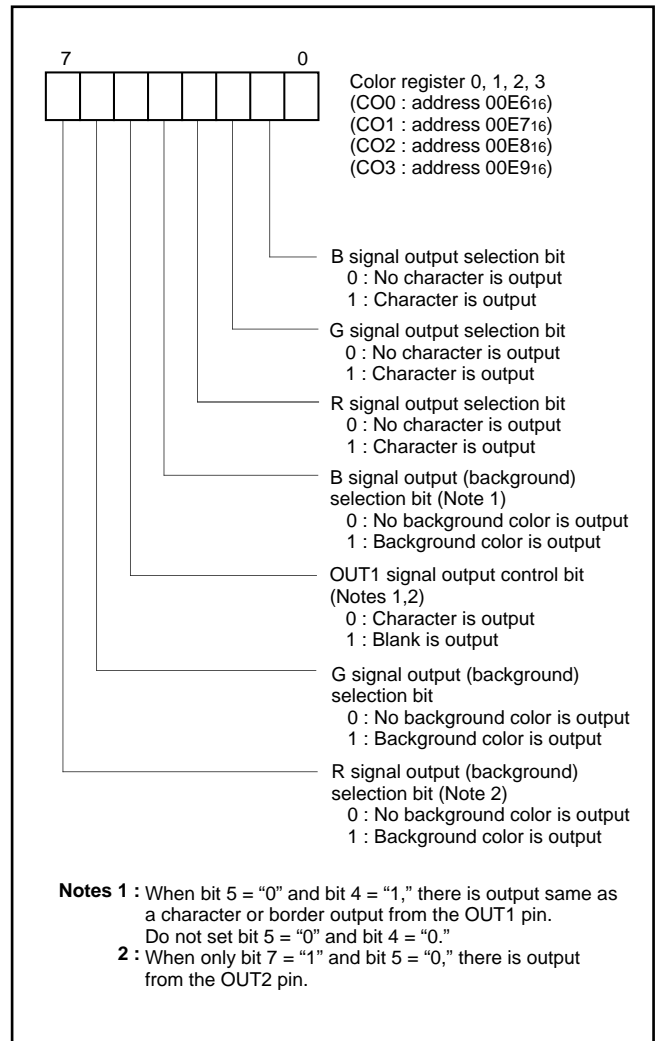


Fig. 46. Structure of color registers

Table 13. Display example of character background coloring (when green is set for a character and blue is set for background color)

Border selection register								Color register								G output	B output	OUT1 output	Character output	OUT2 output
MD ₀	CON ₇	CON ₆	CON ₅	CON ₄	CON ₃	CON ₂	CON ₁	MD ₀	CON ₇	CON ₆	CON ₅	CON ₄	CON ₃	CON ₂	CON ₁					
0	0	X	0	1	0	1	0	(Note 1)									No output			No output (Note 2)
0	1	X	0	1	0	1	0										No output			
0	0	0	1	0	0	1	0										No output			No output (Note 2)
0	0	0	1	1	0	1	0													No output (Note 2)
1	X	X	0	1	0	1	0										No output			No output (Note 2)
1	0	0	1	0	0	1	0										No output			No output (Note 2)
1	0	0	1	1	0	1	0													No output (Note 2)

Notes1 : When CON₅ = "0" and CON₄ = "1," there is output same as a character or border output from the OUT1 pin.

Do not set CON₅ = "0" and CON₄ = "0."

2 : When only CON₇ = "1" and CON₅ = "0," there is output from the OUT2 pin.

3 : The portion "A" in which character dots are displayed is not mixed with any TV video signal.

4 : The wavy-lined arrows in the Table denote video signals.

5 : n : 0 to 3, X : 0 or 1

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(6) Character Border Function

An border of 1 clock (1 dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions. The border is output from the OUT pin. In this case, set bit 5 of a color register to "0" (character is output).

Border can be specified in units of block by using the border selection register (address 00E5₁₆). Figure 47 shows the structure of the border selection register. Table 14 shows the relationship between the values set in the border selection register and the character border function.

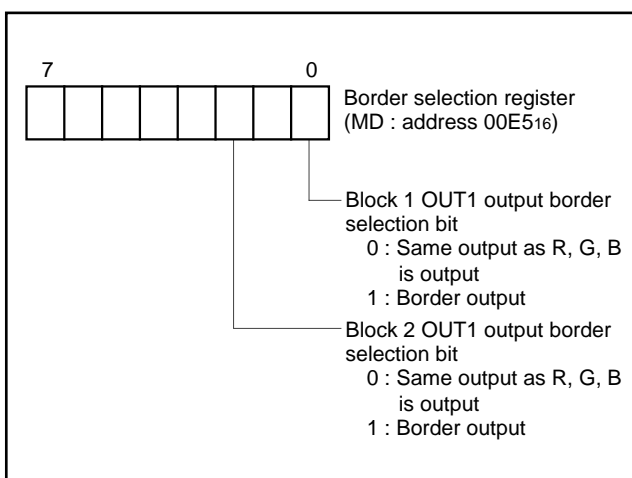


Fig. 47. Structure of border selection register

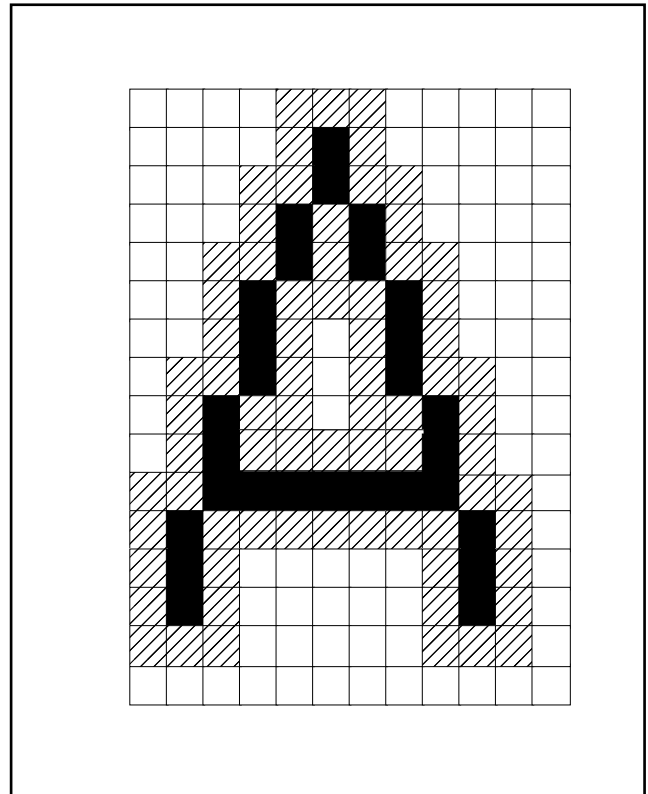


Fig. 48. Example of border

Table 14. Relationship between set value in border selection register and character border function

Border selection register MDn0	Functions	Example of output
0	Ordinary	R, G, B output OUT output
1	Border including character	R, G, B output OUT output

(7) Multiline Display

The M37221EF-XXXSP can ordinarily display 2 lines on the CRT screen by displaying 2 blocks at different vertical positions. In addition, it can display up to 16 lines by using CRT interrupts.

A CRT interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

Note: A CRT interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display with the display control bit of the CRT control register (address 00EA16), a CRT interrupt request does not occur (refer to Figure 49).

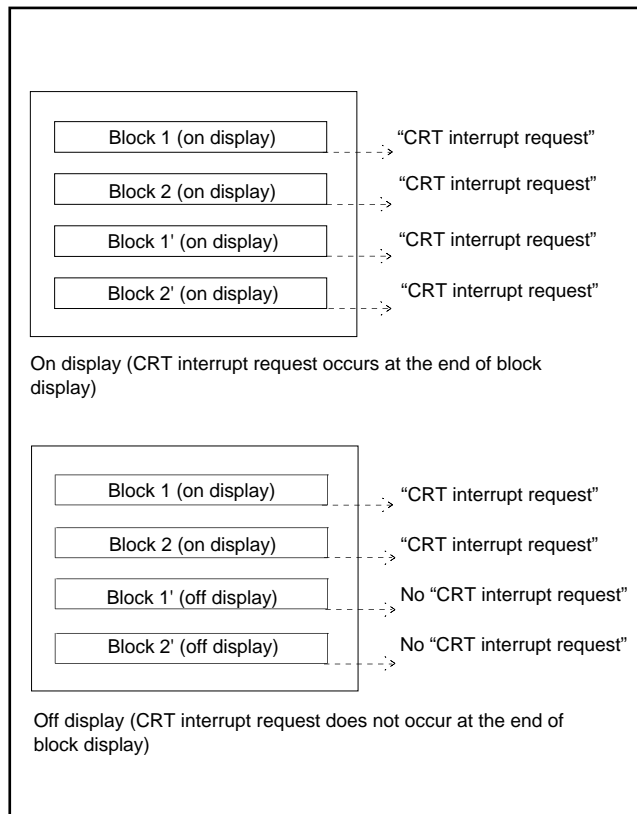


Fig. 49. Timing of CRT interrupt request

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(8) CRT Output Pin Control

The CRT output pins R, G, B, and OUT1 can also function as ports P52, P53, P54 and P55. Set the corresponding bit of the port P5 direction register (address 00CB₁₆) to "0" to specify these pins as CRT output pins, or set it to "1" to specify it as a general-purpose port P5 pins. The OUT2 pin can also function as port P10. Set bit 7 of the CRT control register (address 00EA₁₆) to "0" to specify it as port P10, set it to "1" to specify it as OUT2 pin.

The input polarity of signals HSYNC and VSYNC and output polarity of signals R, G, B, and OUT1 can be specified with the bits of the CRT port control register (address 00EC₁₆). Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity. The structure of the CRT port control register is shown in Figure 50.

(9) Raster Coloring Function

An entire screen (raster) can be colored by setting the bits 5 to 7 of the CRT port control register. Since each of the R, G, and B pins can be switched to raster coloring output, 7 raster colors can be obtained. If the R, G, and B pins have been set to MUTE signal output, a raster coloring signal is output in the part except a no-raster colored character (in Figure 51, a character "O") during 1 horizontal scanning period. This ensures that character colors do not mix with the raster color. In this case, MUTE signal is output from the OUT1 pin. An example in which a magenta character "I" and a red character "O" are displayed with blue raster coloring is shown in Figure 51.

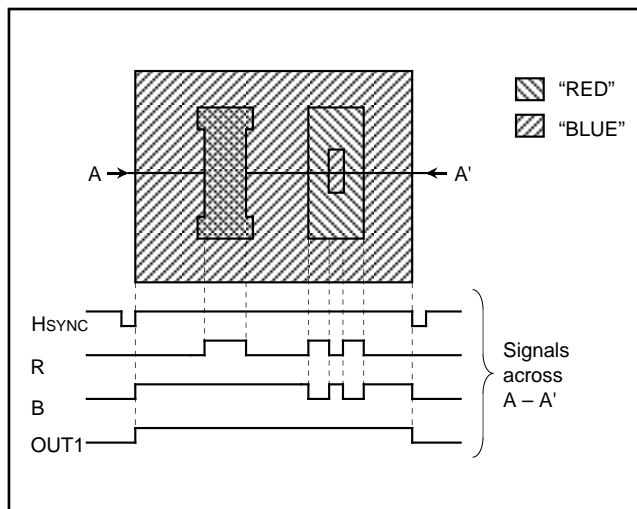


Fig. 51. Example of raster coloring

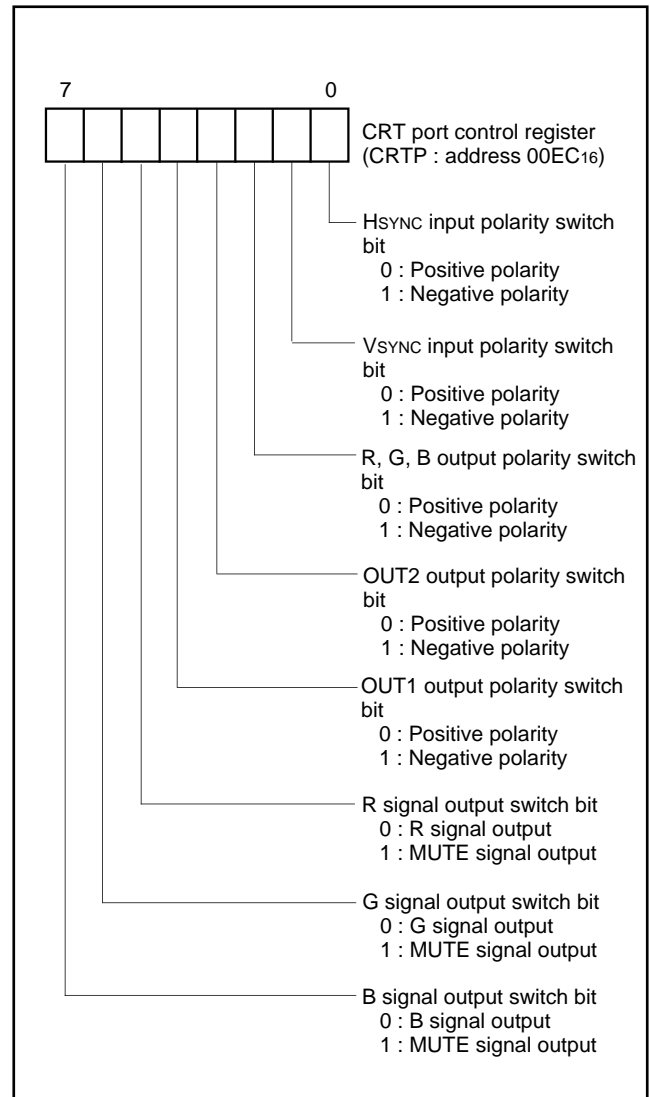


Fig. 50. Structure of CRT port control register

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(10) Clock for Display

As a clock for display to be used for CRT display, it is possible to select one of the following 4 types.

- Main clock supplied from the XIN pin
- Main clock supplied from the XIN pin divided by 1.5
- Clock from the LC or RC supplied from the pins OSC1 and OSC2.
- Clock from the ceramic resonator or quartz-crystal oscillator supplied from the pins OSC1 and OSC2.

This clock for display can be selected for each block by the CRT clock selection register (address 00ED₁₆).

When selecting the main clock, set the oscillation frequency to 8 MHz.

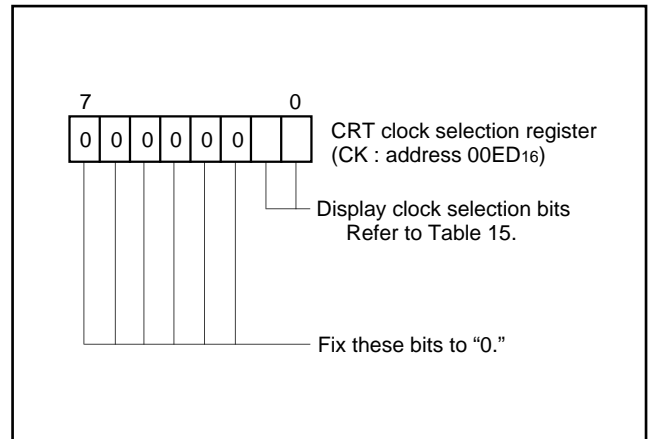


Fig. 52. Structure of CRT clock selection register

Table 15. Set value of CRT clock selection register and clock for display

b1	b0	Functions	
0	0	The clock for display is supplied by connecting RC or LC across the pins OSC1 and OSC2.	
0	1	Since the main clock is used as the clock for display, the oscillation frequency is limited. Because of this, the character size in width (horizontal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports P33 and P34 respectively.	CRT oscillation frequency = $f(XIN)$
1	0		CRT oscillation frequency = $f(XIN)/1.5$
1	1	The clock for display is supplied by connecting the following across the pins OSC1 and OSC2. <ul style="list-style-type: none"> • a ceramic resonator only for CRT display and a feedback resistor • a quartz-crystal oscillator only for CRT display and a feedback resistor (Note) 	

Note: It is necessary to connect other ceramic resonator or quartz-crystal oscillator across the pins XIN and XOUT.

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ROM CORRECTION FUNCTION

This can correct ROM data in ROM (64K bytes). Up to 2 addresses (2 blocks) can be corrected, a program for correction is stored in the ROM memory for correction. The ROM memory for correction is 32 bytes X 2 blocks.

Block 1 : addresses 02C0₁₆ to 02DF₁₆

Block 2 : addresses 02E0₁₆ to 02FF₁₆

Set an address of ROM data to be corrected into the ROM correction address. When the value of the counter matches the ROM data address in the ROM correction address, the main program branches to the program for correction stored in the ROM memory for correction. To return from the program for correction to the main program, the op code and operand of the JMP instruction (total of 3 bytes) is needed at the end of the program for correction. In the case that the blocks 1 and 2 are used in series, the above instruction is not needed at the end of the block 1.

The ROM correction function is controlled by the ROM correction enable register.

- Notes 1 :** Specify the first address (op code address) of each instruction as ROM correction address.
- 2 :** Use the JMP instruction (total of 3 bytes) to return from the main program to the program for correction.
- 3 :** Do not set the same ROM correction address to the blocks 1 and 2.

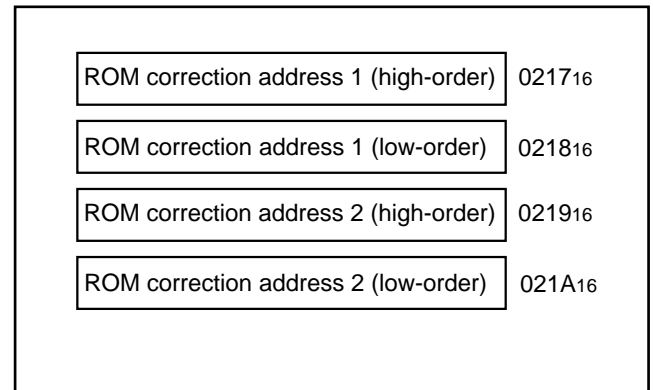


Fig. 53. ROM correction addresses

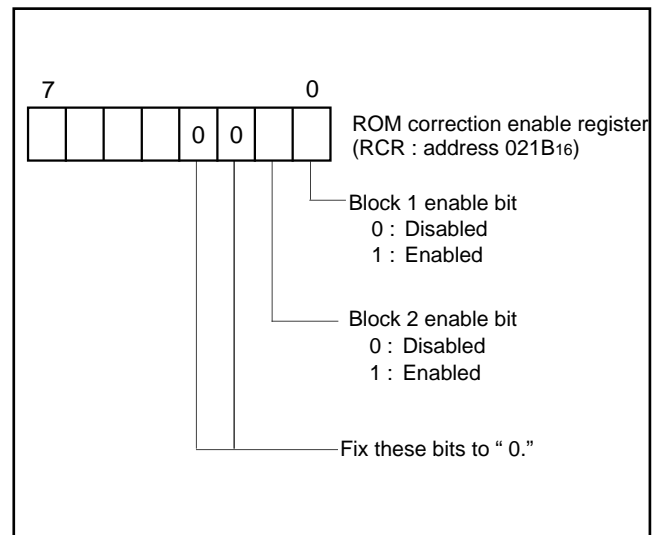


Fig. 54. Structure of ROM correction enable register

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RESET CIRCUIT

The M37221EF-XXXSP is reset according to the sequence shown in Figure 56. It starts the program from the address formed by using the content of address FFFF₁₆ as the high-order address and the content of the address FFFE₁₆ as the low-order address, when the RESET pin is held at "L" level for 2 μs or more while the power source voltage is 5 V ± 10 % and the oscillation of a quartz-crystal oscillator

or a ceramic resonator is stable and then returned to "H" level. The internal state of microcomputer at reset are shown in Figure 57.

An example of the reset circuit is shown in Figure 55.

The reset input voltage must be kept 0.6 V or less until the power source voltage surpasses 4.5 V.

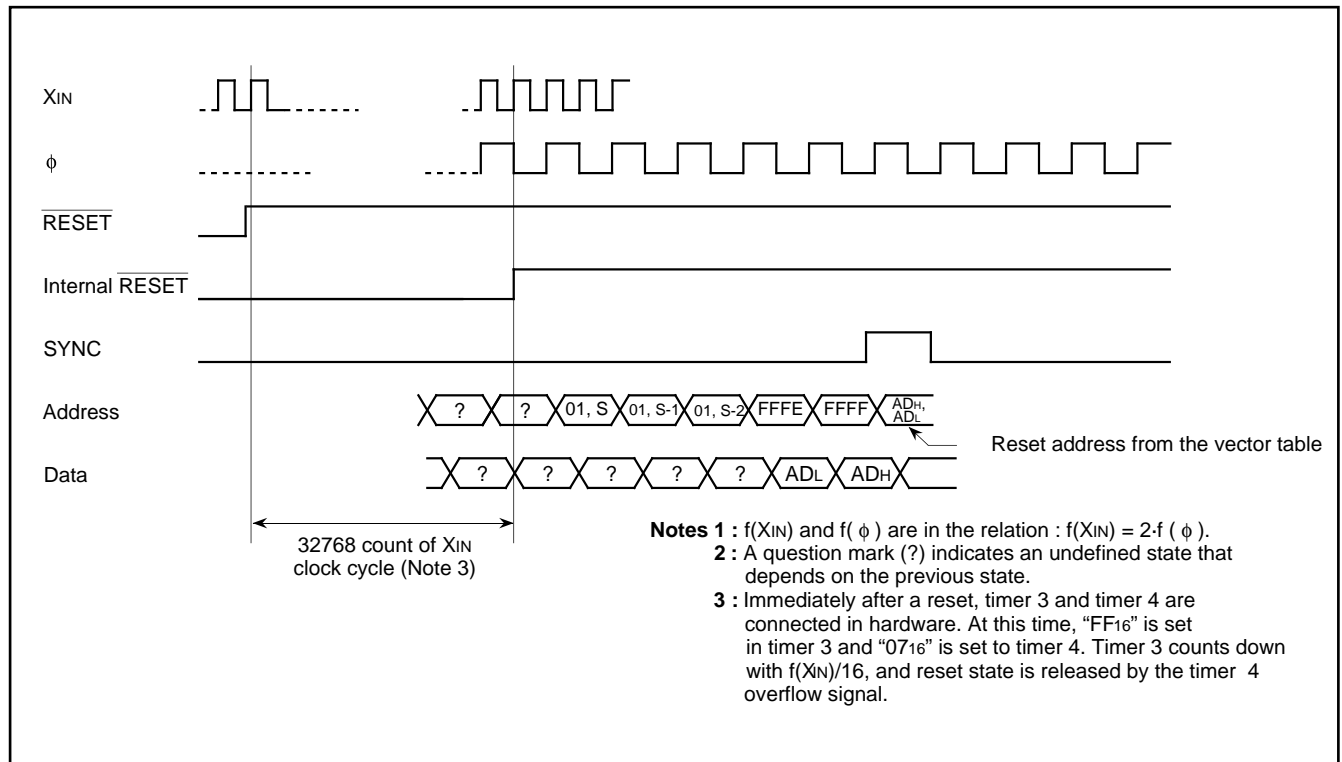


Fig. 56. Reset sequence

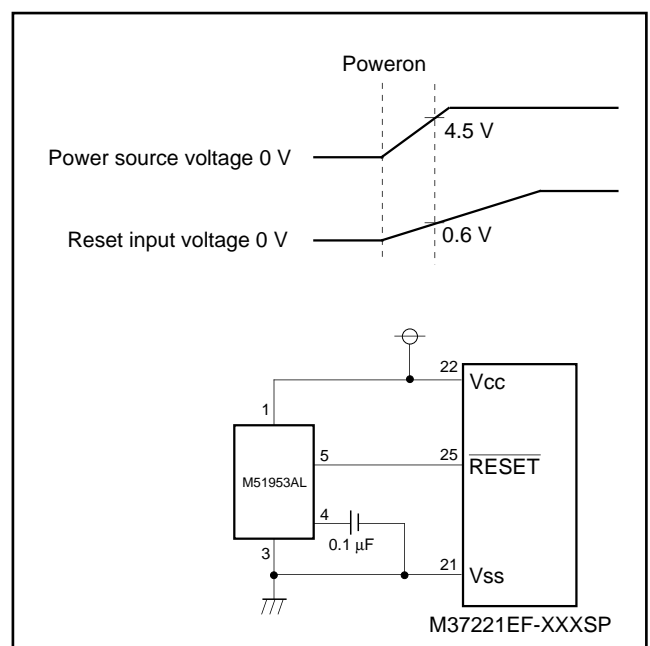


Fig. 55. Example of reset circuit

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	Address	Contents of register		Address	Contents of register
Port P0 direction register	(00C1 ₁₆)	00 ₁₆	CRT control register	(00EA ₁₆)	0XXXXX000
Port P1 direction register	(00C3 ₁₆)	00 ₁₆	CRT port control register	(00EC ₁₆)	00000000
Port P2 direction register	(00C5 ₁₆)	00 ₁₆	CRT clock selection register	(00ED ₁₆)	XXXXXXXX00
Port P3 direction register	(00C7 ₁₆)	XXXXXX000	A-D control register 1	(00EE ₁₆)	XXXX*XX00
Port P5	(00CA ₁₆)	XX*****X	A-D control register 2	(00EF ₁₆)	XX000000
Port P5 direction register	(00CB ₁₆)	XX0000XX	Timer 1	(00F0 ₁₆)	FF ₁₆
Port P3 output mode control register	(00CD ₁₆)	XXXXX0000	Timer 2	(00F1 ₁₆)	07 ₁₆
DA-L register	(00CF ₁₆)	XX*****	Timer 3	(00F2 ₁₆)	FF ₁₆
PWM output control register 1	(00D5 ₁₆)	00 ₁₆	Timer 4	(00F3 ₁₆)	07 ₁₆
PWM output control register 2	(00D6 ₁₆)	XXXX000X	Timer 12 mode register	(00F4 ₁₆)	XXXX00000
I ² C address register	(00D8 ₁₆)	00 ₁₆	Timer 34 mode register	(00F5 ₁₆)	XX000000
I ² C status register	(00D9 ₁₆)	0001000*	Interrupt input polarity register	(00F9 ₁₆)	XX000XXXX
I ² C control register	(00DA ₁₆)	00 ₁₆	CPU mode register	(00FB ₁₆)	XXXXXXXX1XX
I ² C clock control register	(00DB ₁₆)	00 ₁₆	Interrupt request register 1	(00FC ₁₆)	00000000
Serial I/O mode register	(00DC ₁₆)	X0000000	Interrupt request register 2	(00FD ₁₆)	XXXX0XX00
DA1 conversion register	(00DE ₁₆)	XX*****	Interrupt control register 1	(00FE ₁₆)	00000000
DA2 conversion register	(00DF ₁₆)	XX*****	Interrupt control register 2	(00FF ₁₆)	XXXX0XX00
Horizontal register	(00E0 ₁₆)	XX000000	ROM correction address 1 (high-order)	(0217 ₁₆)	00 ₁₆
Vertical position register 1	(00E1 ₁₆)	XX*****	ROM correction address 1 (low-order)	(0218 ₁₆)	00 ₁₆
Vertical position register 2	(00E2 ₁₆)	XX*****	ROM correction address 2 (high-order)	(0219 ₁₆)	00 ₁₆
Character size register	(00E4 ₁₆)	XXXXX*****	ROM correction address 2 (low-order)	(021A ₁₆)	00 ₁₆
Border selection register	(00E5 ₁₆)	XXXXXX*XX*	ROM correction enable register	(021B ₁₆)	XXXXXXXX00
Color register 0	(00E6 ₁₆)	0000000X	Processor status register	(PS)	* ** * * 1 * *
Color register 1	(00E7 ₁₆)	0000000X	Program counter	(PCH)	Contents of addressFFFF ₁₆
Color register 2	(00E8 ₁₆)	0000000X		(PCL)	Contents of addressFFFE ₁₆
Color register 3	(00E9 ₁₆)	0000000X			

Note : The contents of all other registers and RAM are undefined at reset, so set their initial values.

* : Undefined

X : Unused bit

Fig. 57. Internal state of microcomputer at reset

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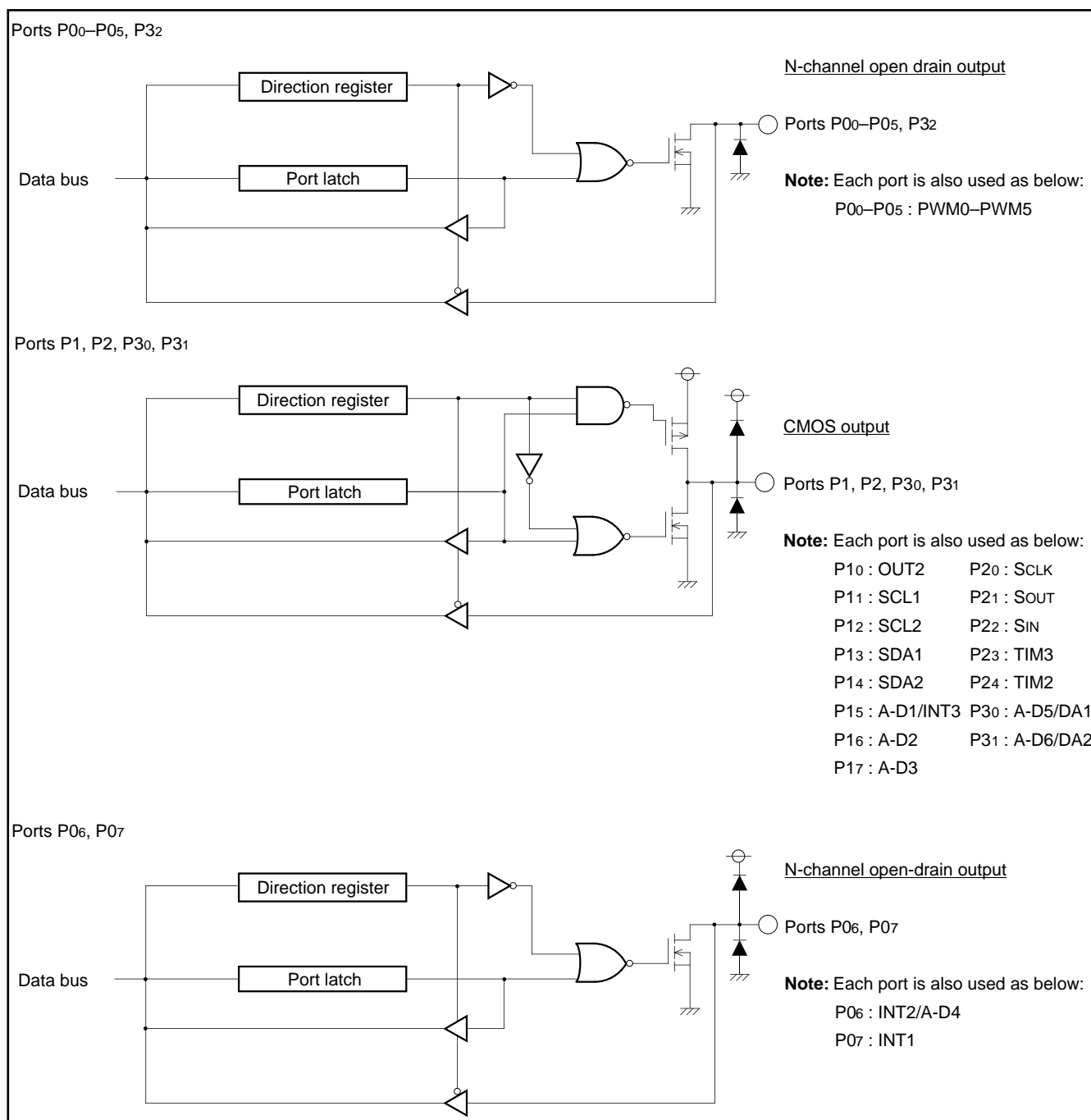


Fig. 58. I/O pin block diagram (1)

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with ON-SCREEN DISPLAY CONTROLLER

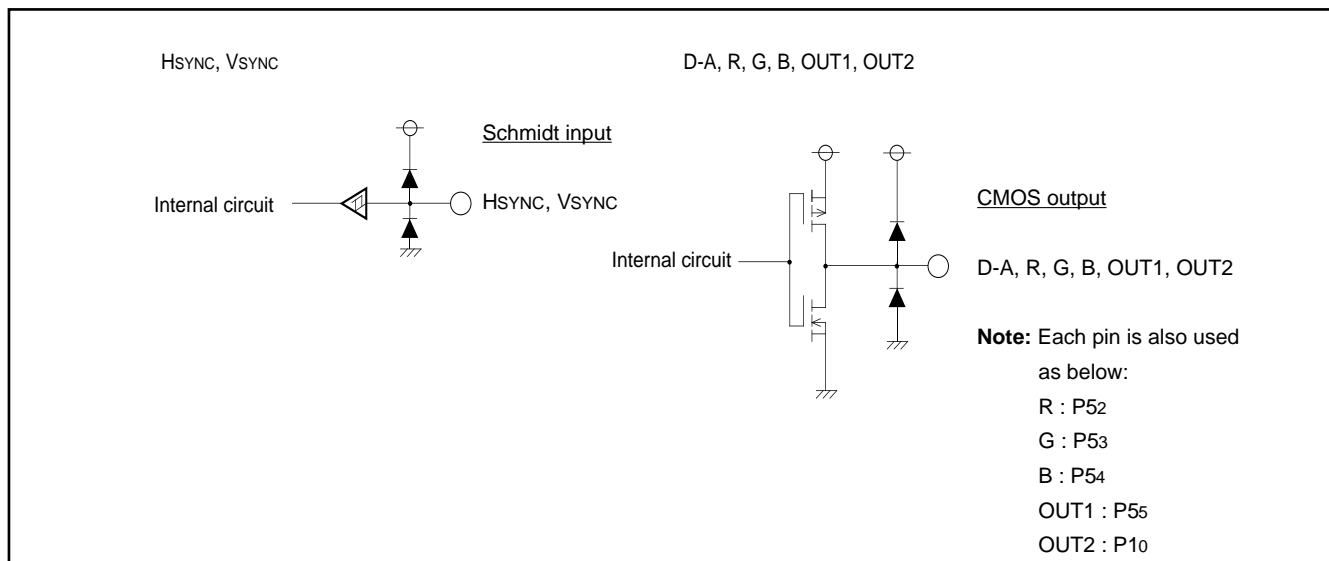


Fig. 59. I/O pin block diagram (2)

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CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 62. When the STP instruction is executed, the internal clock stops at "H" level. At the same time, timers 3 and 4 are connected in hardware and "FF16" is set in the timer 3, "0716" is set in the timer 4. Select $f(X_{IN})/16$ as the timer 3 count source (set bit 0 of the timer 34 mode register to "0" before the execution of the STP instruction). And besides, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction). The oscillator restarts when external interrupt is accepted, however, the internal clock keeps its "H" level until timer 4 overflows. Because this allows time for oscillation stabilizing when a ceramic resonator or a quartz-crystal oscillator is used. When the WIT instruction is executed, the internal clock stops in the "H" level but the oscillator continues running. This wait state is released when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once. When returning from the stop or the wait state, to accept an interrupt, set the corresponding interrupt enable bit to "1" before executing the STP or the WIT instructions.

Note: In the wait mode, the following interrupts are invalid.

- (1) VSYNC interrupt
- (2) CRT interrupt
- (3) $f(X_{IN})/4096$ interrupt
- (4) Timer 1 interrupt using $f(X_{IN})/4096$ as count source
- (5) Timer 2 interrupt using P24/TIM2 pin input as count source
- (6) Timer 3 interrupt using P23/TIM3 pin input as count source
- (7) Timer 4 interrupt using $f(X_{IN})/2$ as count source
- (8) Multi-master I²C-BUS interface interrupt

The circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 60. Use the circuit constants in accordance with the resonator manufacture's recommended values. The circuit example with external clock input is shown in Figure 61. Input the clock to the X_{IN} pin, and open the X_{OUT} pin.

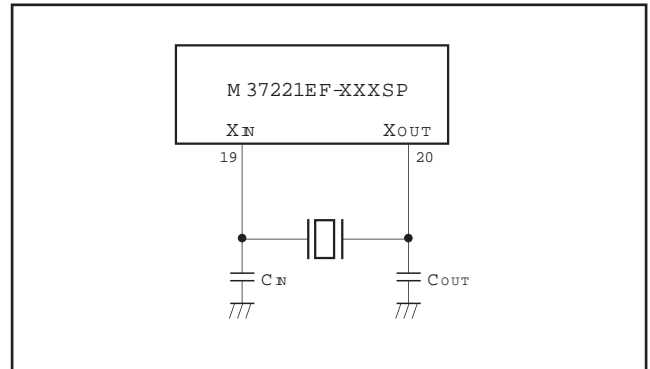


Fig. 60. Ceramic resonator circuit example

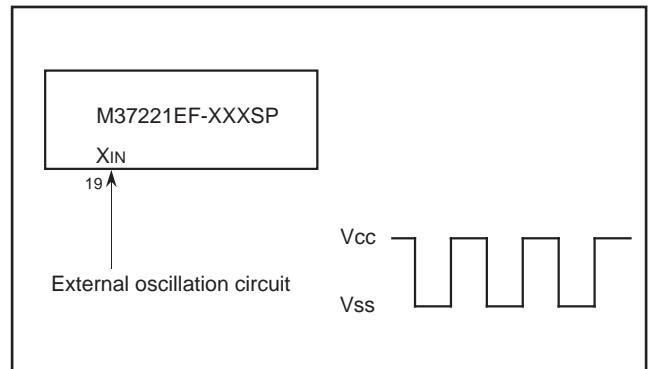


Fig. 61. External clock input circuit example

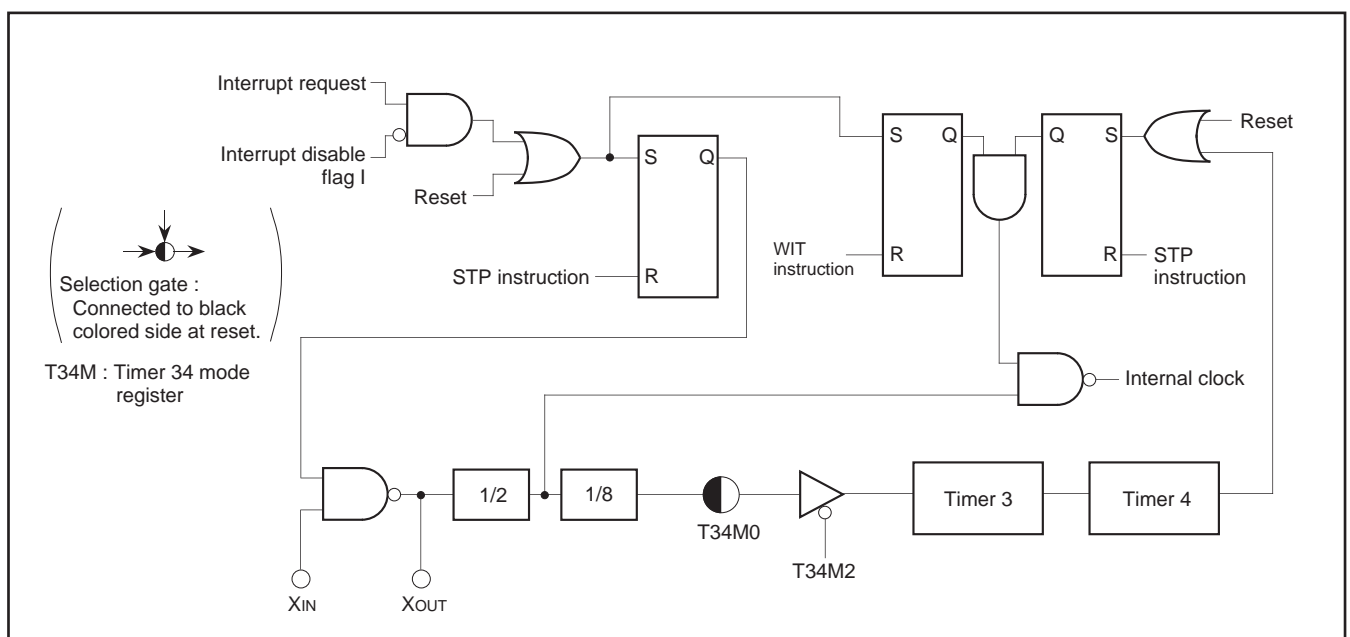


Fig. 62. Clock generating circuit block diagram

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DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has a built-in clock oscillation circuits, so that a clock for CRT display can be obtained simply by connecting an LC, an RC, a ceramic resonator or a quartz-crystal oscillator circuit across the pins OSC 1 and OSC 2. Select the clock for display with bits 0 and 1 of the CRT clock selection register (address 00ED16).

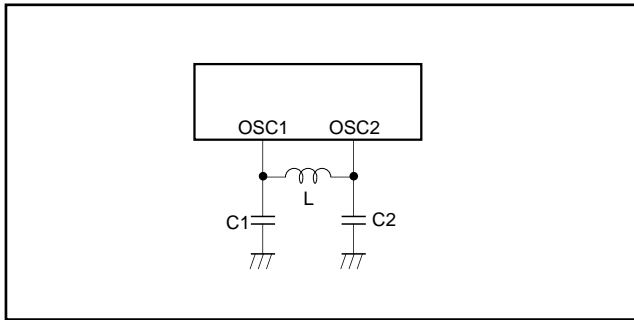


Fig. 63. Display oscillation circuit

AUTO-CLEAR CIRCUIT

When power source is supplied, the auto-clear function can be performed by connecting the following circuit to the RESET pin.

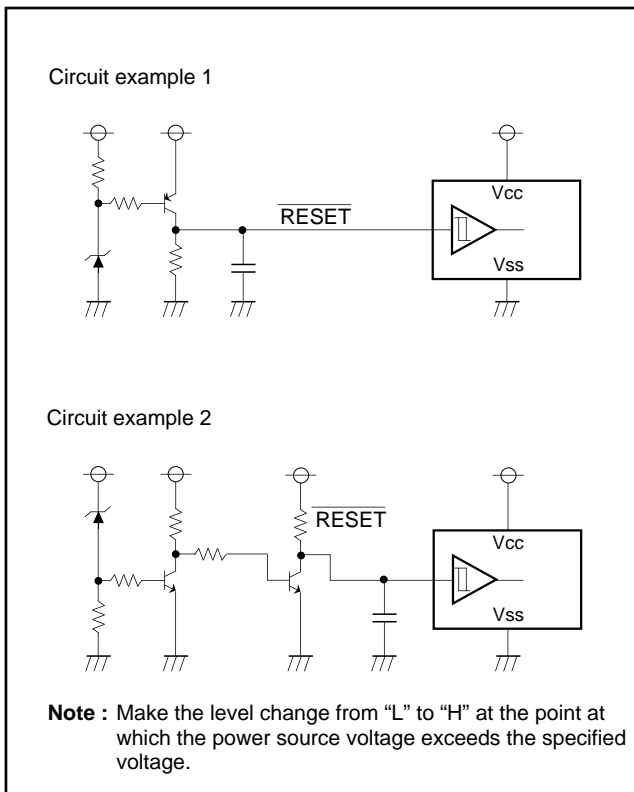


Fig. 64. Auto-clear circuit example

ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to the SERIES 740 <Software> User's Manual for details.

MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to the SERIES 740 <Software> User's Manual for details.

PROGRAMMING NOTES

- (1) The divide ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- (4) An NOP instruction is needed immediately after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1 \mu\text{F}$) directly between the Vcc pin-Vss pin and the Vcc pin-CNVss pin using a thick wire.

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PROM Programming Method

The built-in PROM of the One Time PROM version (blank) and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37221EFSP	PCA7408

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 65 is recommended to verify programming.

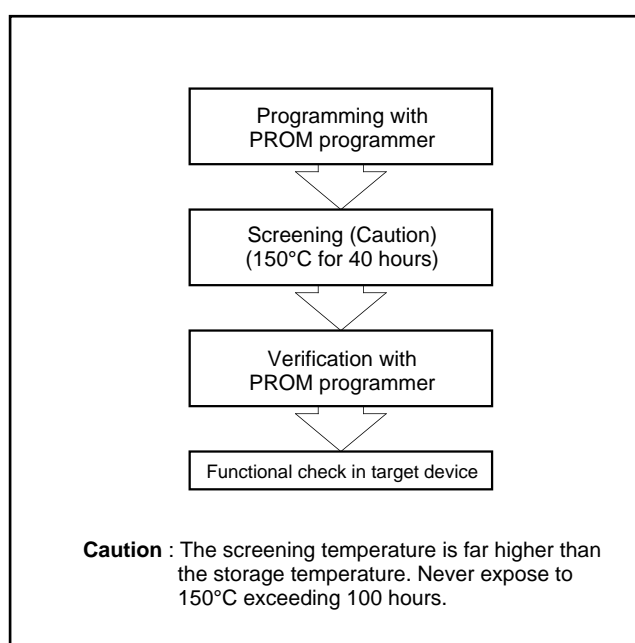


Fig. 65. Programming and testing of One Time PROM version

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage VCC	All voltages are based on Vss. Output transistors are cut off.	-0.3 to 6	V
Vi	Input voltage CNVss		-0.3 to 6	V
Vi	Input voltage P00-P07,P10-P17, P20-P27, P30-P34, OSC1, XIN, HSYNC, VSYNC, RESET		-0.3 to Vcc + 0.3	V
Vo	Output voltage P06, P07, P10-P17, P20-P27, P30-P32, R, G, B, OUT1, D-A, XOUT, OSC2		-0.3 to Vcc + 0.3	V
Vo	Output voltage P00-P05		-0.3 to 13	V
IOH	Circuit current R, G, B, OUT1, P10-P17, P20-P27, P30, P31, D-A		0 to 1 (Note 1)	mA
IOL1	Circuit current R, G, B, OUT1, P06, P07, P10, P15-P17, P20-P23, P30-P32, D-A		0 to 2 (Note 2)	mA
IOL2	Circuit current P11-P14		0 to 6 (Note 2)	mA
IOL3	Circuit current P00-P05		0 to 1 (Note 2)	mA
IOL4	Circuit current P24-P27		0 to 10 (Note 3)	mA
Pd	Power dissipation	Ta = 25 °C	550	mW
Topr	Operating temperature		-10 to 70	°C
Tstg	Storage temperature		-40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -10 °C to 70 °C, Vcc = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Power source voltage (Note 4), During CPU, CRT operation	4.5	5.0	5.5	V
Vss	Power source voltage	0	0	0	V
VIH1	"H" input voltage P00-P07,P10-P17, P20-P27, P30-P34, SIN, SCLK, HSYNC, VSYNC, RESET, XIN, OSC1, TIM2, TIM3, INT1, INT2, INT3	0.8Vcc		Vcc	V
VIH2	"H" input voltage SCL1, SCL2, SDA1, SDA2 (When using I ² C-BUS)	0.7Vcc		Vcc	V
VIL1	"L" input voltage P00-P07,P10-P17, P20-P27, P30-P34	0		0.4 Vcc	V
VIL2	"L" input voltage SCL1, SCL2, SDA1, SDA2 (When using I ² C-BUS)	0		0.3 Vcc	V
VIL3	"L" input voltage HSYNC, VSYNC, RESET, TIM2, TIM3, INT1, INT2, INT3, XIN, OSC1, SIN, SCLK	0		0.2 Vcc	V
IOH	"H" average output current (Note 1) R, G, B, OUT1, D-A, P10-P17, P20-P27, P30, P31			1	mA
IOL1	"L" average output current (Note 2) R, G, B, OUT1, D-A, P06, P07, P10, P15-P17, P20-P27, P30-P32			2	mA
IOL2	"L" average output current (Note 2) P11-P14			6	mA
IOL3	"L" average output current (Note 2) P00-P05			1	mA
IOL4	"L" average output current (Note 3) P24-P27			10	mA
fCPU	Oscillation frequency (for CPU operation) (Note 5) XIN	7.9	8.0	8.1	MHz
fCRT	Oscillation frequency (for CRT display) (Note 5) OSC1	5.0		8.0	MHz
fhs1	Input frequency TIM2, TIM3			100	kHz
fhs2	Input frequency SCLK			1	MHz
fhs3	Input frequency SCL1, SCL2			400	kHz

Notes 1: The total current that flows out of the IC must be 20 mA (max.).

2: The total input current to IC (IOL1 + IOL2 + IOL3) must be 30 mA or less.

3: The total average input current for ports P24-P27 to IC must be 20 mA or less.

4: Connect 0.1 μF or more capacitor externally across the power source pins Vcc-Vss so as to reduce power source noise. Also connect 0.1 μF or more capacitor externally across the pins Vcc-CNVss.

5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.

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ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
I _{CC}	Power source current	System operation	V _{CC} = 5.5 V, f(X _{IN}) = 8 MHz	CRT OFF		20	40	mA
				CRT ON		30	60	
		Stop mode	V _{CC} = 5.5 V, f(X _{IN}) = 0				300	μA
V _{OH}	"H" output voltage	R, G, B, OUT1, D-A, P10-P17, P20-P27, P30, P31	V _{CC} = 4.5 V I _{OH} = -0.5 mA		2.4			V
V _{OL}	"L" output voltage	R, G, B, OUT1, D-A, P00-P07, P10, P15-P17, P20-P23, P30-P32	V _{CC} = 4.5 V I _{OL} = 0.5 mA				0.4	V
	"L" output voltage	P11-P14	V _{CC} = 4.5 V	I _{OL} = 3 mA			0.4	
				I _{OL} = 6 mA			0.6	
	"L" output voltage	P24-P27	V _{CC} = 4.5 V I _{OL} = 10.0 mA				3.0	
V _{T+} -V _{T-}	Hysteresis	RESET	V _{CC} = 5.0 V			0.5	0.7	V
	Hysteresis (Note)	HSYNC, VSYNC, TIM2, TIM3, INT1, INT2, INT3, SCL1, SCL2, SDA1, SDA2, SIN, SCLK	V _{CC} = 5.0 V			0.5	1.3	
I _{IzH}	"H" input leak current	RESET, P00-P07, P10-P17, P20-P27, P30-P34, HSYNC, VSYNC	V _{CC} = 5.5 V V _I = 5.5 V				5	μA
I _{IzL}	"L" input leak current	RESET, P00-P07, P10-P17, P20-P27, P30-P34, HSYNC, VSYNC	V _{CC} = 5.5 V V _I = 0 V				5	μA
I _{OZH}	"H" output leak current	P00-P05	V _{CC} = 5.5 V V _O = 12 V				10	μA
R _{BS}	I ² C-BUS-BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V _{CC} = 4.5 V				130	Ω

Note: P06, P07, P15, P23, P24 have the hysteresis when these pins are used as interrupt input pins or timer input pins. P20-P22 have the hysteresis when these pins are used as serial I/O pins. P11-P14 have the hysteresis when these pins are used as multi-master I²C-BUS interface pins.

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A-D COMPARATOR CHARACTERISTICS

(VCC = 5 V ± 10 %, VSS = 0 V, f(XIN) = 8 MHz, Ta = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Absolute accuracy		0	±1	±2	LSB

Note: When VCC = 5 V, 1 LSB = 5/64 V.

D-A CONVERTER CHARACTERISTICS

(VCC = 5 V ± 10 %, VSS = 0 V, f(XIN) = 8 MHz, Ta = -10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Absolute accuracy				2	%
tsu	Setting time				3	μs
RO	Output resistor		1	2.5	4	kΩ

MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
tBUF	Bus free time	4.7		1.3		μs
tHD:STA	Hold time for START condition	4.0		0.6		μs
tLOW	"L" period of SCL clock	4.7		1.3		μs
tR	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
tHD:DAT	Data hold time	0		0	0.9	μs
tHIGH	"H" period of SCL clock	4.0		0.6		μs
tF	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
tsu:DAT	Data set-up time	250		100		ns
tsu:STA	Set-up time repeated for START condition	4.7		0.6		μs
tsu:STO	Set-up time for STOP condition	4.0		0.6		μs

Note: Cb = total capacitance of 1 bus line

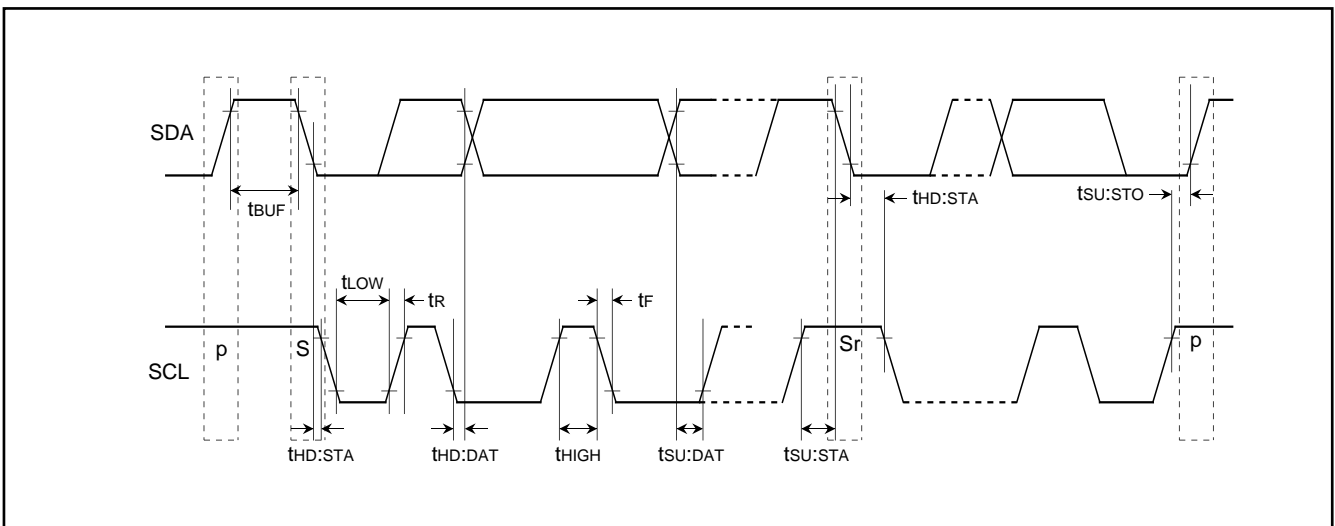
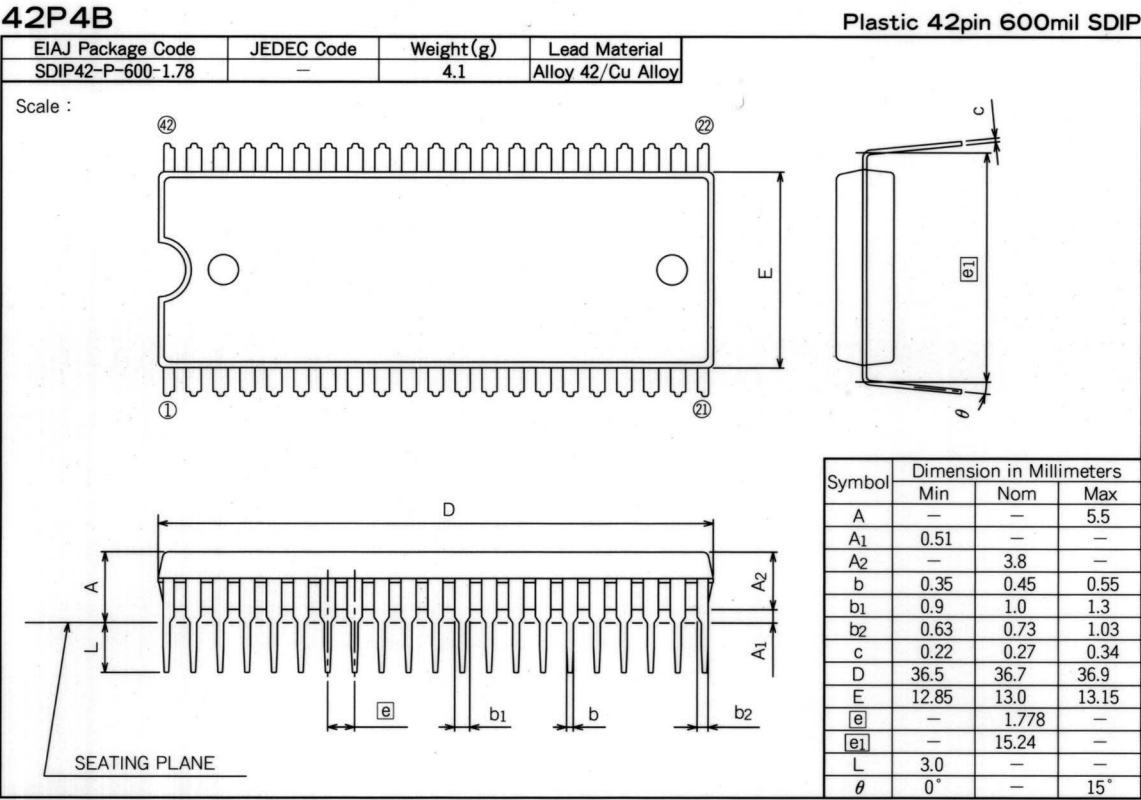


Fig. 66. Definition diagram of timing on multi-master I²C-BUS

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PACKAGE OUTLINE



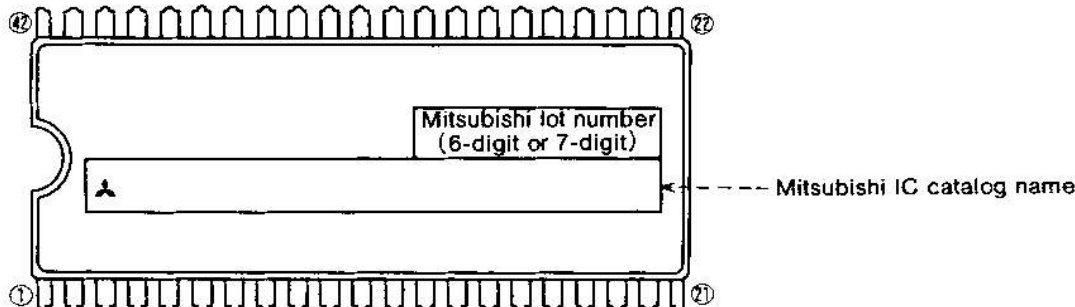
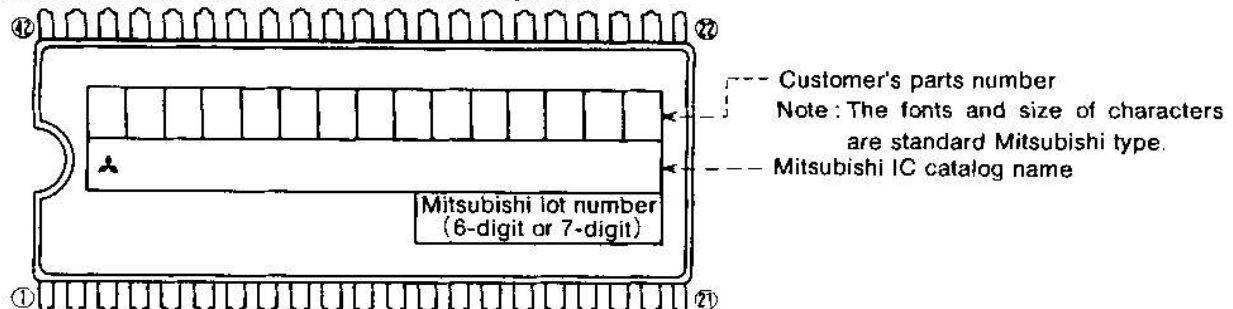
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Mitsubishi IC catalog name

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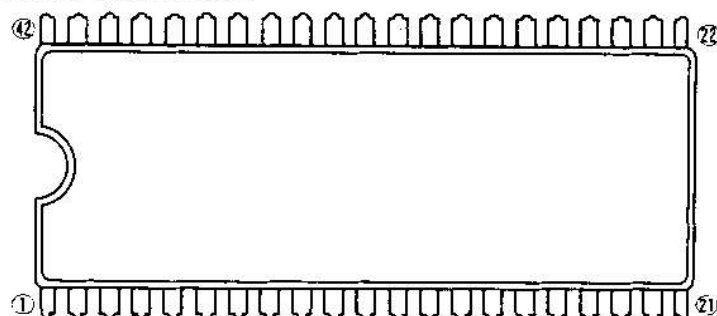
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